

# PolarFire® FPGAs and SoC FPGAs



[microchip.com/FPGA](http://microchip.com/FPGA)

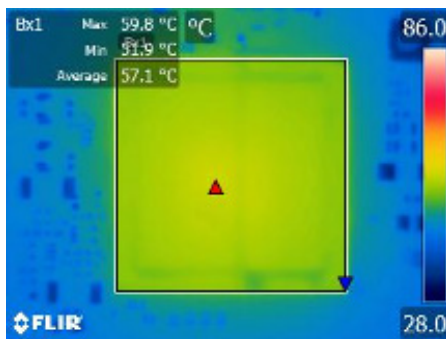


## PolarFire FPGAs and SoC FPGAs Consume the Lowest Total Power

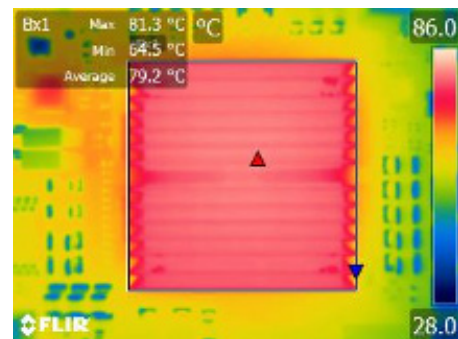
PolarFire FPGAs and SoC FPGAs deliver up to two times the performance per watt compared to competitive devices.

The thermal images below show the power and heat dissipation when identical designs are run on competitive products.

## Superior Power and Thermal Performance

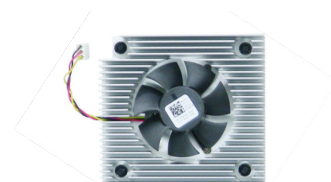
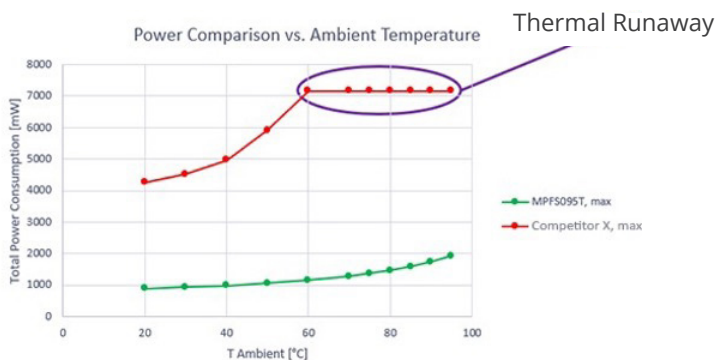


Microchip PolarFire FPGA 3.5W, 59.8°C, 24.2 FIT, 28 nm



Competitor X FPGA, 6.0W, 81.3°C, 96.3 FIT, 16 nm

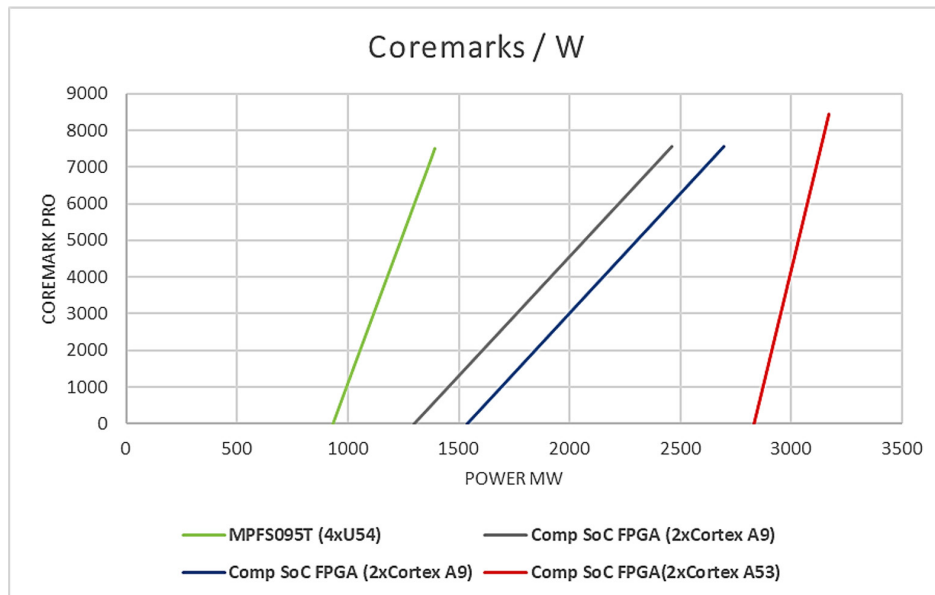
PolarFire FPGAs and SoC FPGAs demonstrate a far superior thermal performance over the operating temperature range. The following charts show a stable power and thermal performance of PolarFire SoC FPGAs while a competing SoC FPGA demonstrates a thermal runaway at a 60°C ambient temperature. Failure In Time (FIT) rate grows exponentially over temperature; the low power consumption of PolarFire SoCs and FPGAs deliver superior FIT rates.



Eliminating fans lowers cost and increases system reliability



PolarFire SoC FPGAs deliver significant power savings while outperforming SRAM-based SoC FPGAs over the operating temperature range. While consuming 1.3W, PolarFire SoC FPGAs deliver a CoreMark® score of 6000 while competing SRAM-based SoC FPGAs deliver a CoreMark score of 0.



At worst case process and temperature

Source: Published power estimations of FPGA static and processor subsystem power.

### Low Power Advantages

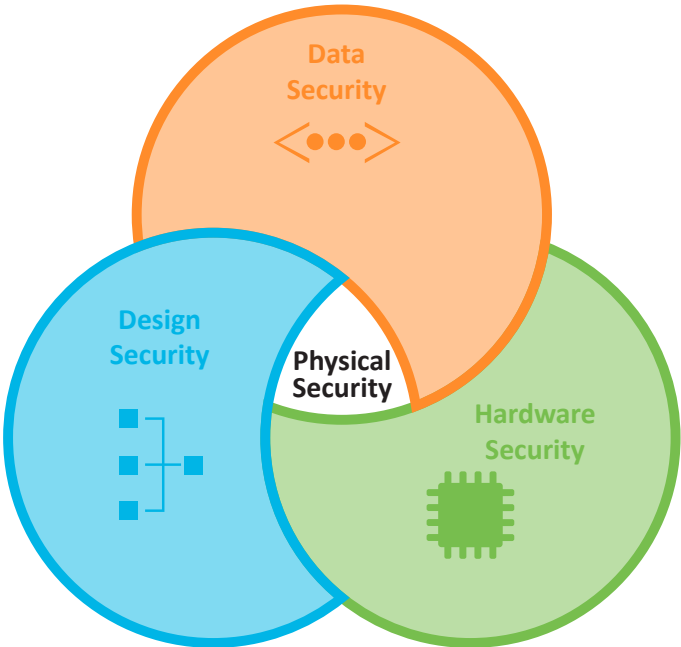
- Save up to \$1.5/W (fan-less and heatsink-less designs)
- Enable power- and thermal-constrained applications
- Create smaller industrial designs
- Achieve lower FIT rates with lower thermals



### Defense Grade Security

### Cybersecurity is the #1 Concern for Connected Devices on the Network Edge

It is not enough for today's demanding applications to meet the functional requirements of their design—they must do so in a secured way. Security starts during silicon manufacturing and continues through system deployment and operations. Our PolarFire SoC FPGAs represent the industry's most advanced secure programmable FPGAs.



#### Information Assurance

- Built-in User Crypto Accelerators
- Built-in Random Number Generator
- PUF Protected Key Storage

#### Anti-Tamper

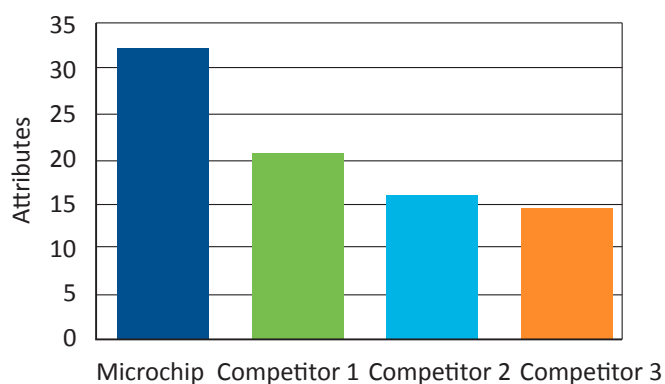
- 32 built-in Anti-Tamper Flags
- Bitstream Security
- 14 Device Locks
- Secure Non-Volatile Memory

#### Trust

- Cryptographically Controlled Supply Chain
- NIST Certified Crypto Accelerators
- PUF and Hardware Root of Trust
- Licensed Patent Protected DPA Resistance

Security Features	PolarFire® SoC	Competitor 1	Competitor 2	Competitor 3
<b>TRNG</b>	Hard-IP (SP800-90A CTR_DRBG-256; SP800-90B (draft) NRBG)	☒	☒	Soft-IP
<b>AES</b>	AES-128/192/256 (ECB, CBC, CTR, OFB, CFB, GCM, KeyWrap)	AES-256 (CBC)	AES-256 (CBC)	AES-256 (ECB, GCM)
<b>SHA</b>	SHA-1/224/256/384/512, Key Tree	SHA-256	SHA-256	SHA-384
<b>HMAC</b>	HMAC-SHA-1/224/256/384/512; GMAC-AES; CMAC-AES	HMAC-SHA2-256	HMAC-SHA2-256	☒
<b>RSA</b>	SigGen (ANSI X9.31, PKCS v1.5), SigVer (ANSI X9.31, PKCS v1.5)-1024/1536/2048/3072/4096	Soft-RSA -(2048) SigGen(PKCS v1.5), SigVer (PKCS v1.5)	Soft-RSA -(2048) SigGen(PKCS v1.5), SigVer (PKCS v1.5)	Software library - RSA primitive (2048)
<b>ECDSA</b>	KeyGen, KeyVer, SigGen & SigVer - NIST & Brainpool (P256/384/521) KAS - ECC CDH, PKG, PKV	☒	☒	☒
<b>FFC</b>	KAS - DH, DSA SigGen & SigVer (1024/1536/2048/3072/4096)	☒	☒	☒
<b>Tamper Sense</b>	Voltage, Temperature, Clock Frequency, Clock Glitch, Active Mesh	☒	☒	Only Voltage & Temperature
<b>PUF</b>	PUF protection for Secure Key storage (Secure Boot and Data communication)	☒	☒	For secure boot key
<b>Bitstream Protection</b>	DPA resistant Encrypted bit-stream programming	☒	☒	✓
<b>DPA Resistance</b>	DPA resistant hard crypto co-processor supporting all above Crypto algorithms	☒	☒	☒
<b>Memory Separation</b>	Physical Memory Protection (PMP)	ARM Trust Zone	ARM Trust Zone	ARM Trust Zone

## Physical Security Attributes



## Information Assurance

- Robust suite of encryption algorithms including CMAC, ECC, FCC, GMAC, IFC, KEYTREE and NRBG

## Anti-Tamper

- Clock Glitch Detection to prevent fault injection attacks
- Bitstream Versioning to protect IP and manage updates
- Memory Separation by Physical Memory Protection
- Device Locks: User Security Locks, Programming Locks, Debug Locks, Permanent Locks

## Trusted Hardware

- Active Mesh for resilient hardware protection
- Unique digital fingerprint through PUF
- HWRoT for secure and verifiable chain of trust



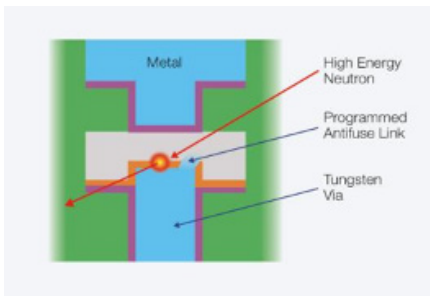
## Exceptional Reliability

Microchip is a proven leader of reliable FPGAs and SoCs for aerospace and defense applications. We extend such reliability to commercial, industrial and automotive applications by implementing Single-Event Upset (SEU) immunity across all our products.

## Features of Error-Free, SEU-Immune Fabric Configuration

- ZeroFIT SEU neutron-immune FPGA configuration
- No need to detect configuration errors
- No scrubbing or TMR required
- Block RAM with ECC
- Lower cost
- Built-in SECEDED on 33-bit word
- System controller suspend mode for safety-critical applications
- SECEDED protection in all MSS memories on PolarFire SoC FPGAs

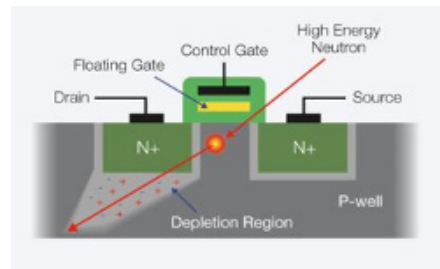
### Antifuse FPGAs



Antifuses have a permanently-programmed metallic link, which cannot be altered by energetic particles or other radiation.



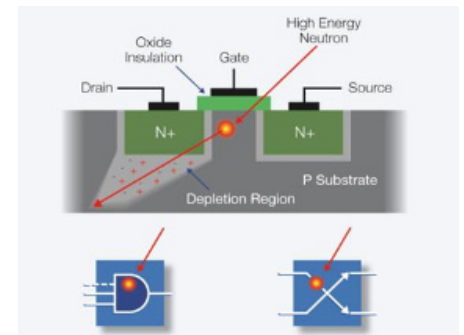
### Nonvolatile FPGAs



High energy particles (atmospheric neutrons, heavy ions in space) are unable to generate sufficient charge to cause the floating gate to erroneously change state.



### SRAM FPGAs



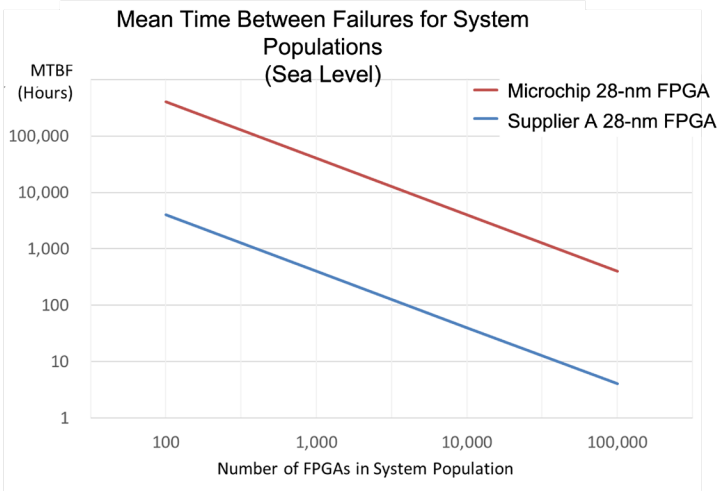
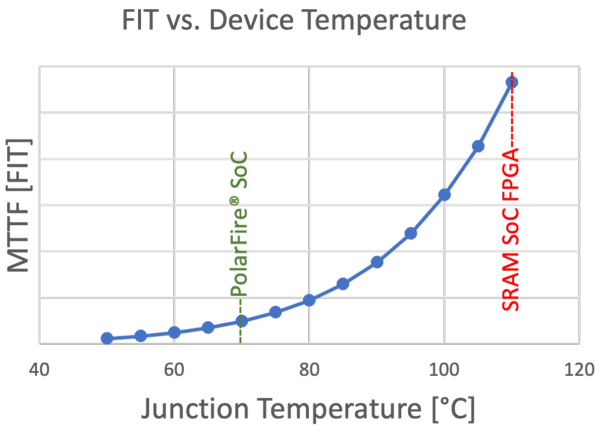
Incoming neutron causes firm error in logic modules leading to





### Exceptional Reliability

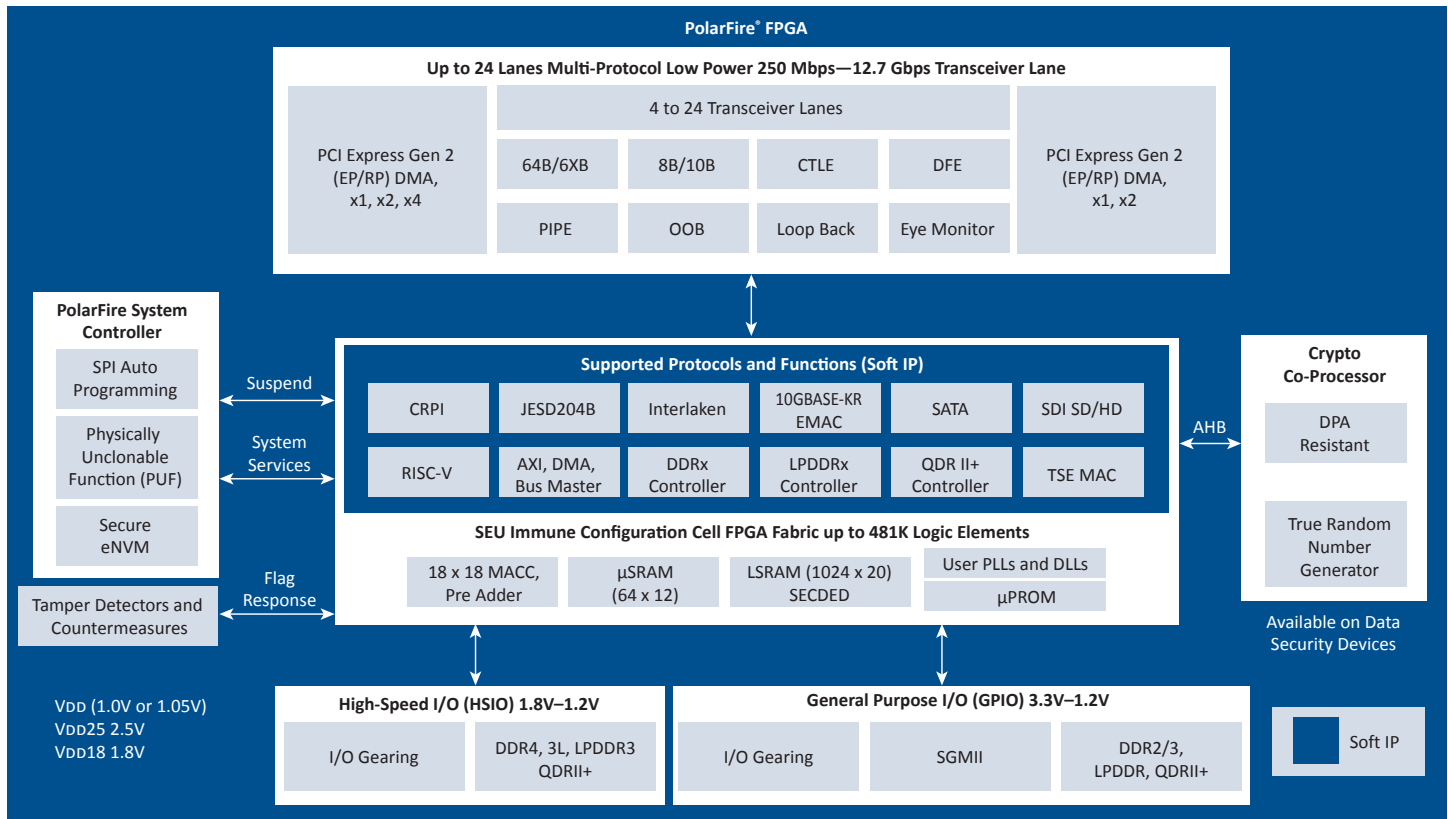
The SEU immunity and low power consumption of PolarFire SoCs and FPGAs offer lower Failure In Time (FIT) rates, enhancing system reliability. The chart below of FIT versus device temperature illustrates how junction temperature affects failures over time and that the low power consumption of PolarFire SoC FPGAs compared to the power consumption of the competition results in significantly lower failures. When considering the Mean Time Between Failures (MTBF) in a product in mass production, a PolarFire SoC FPGA-based product would have a superior MTBF, reducing costs and elevating your reputation..



## PolarFire FPGAs: Low-Power, Secure and Reliable Mid-Range FPGA Platforms

Take advantage of the following features:

- Logic density of 48k to 481 kLE
- Four-input Look-Up Table (LUT) with a fractureable D-type flip-flop
- Up to 24 12.7-Gbps SerDes ports
- Integrated dual PCIe® for up to four Gen 2 Endpoint (EP) and Root Port (RP) designs
- High-speed I/O (HSIO) up to 1600 Mbps DDR4, 1333 Mbps DDR3L and 1333 Mbps LPDDR3/DDR3 memories
- LVDS with I/O gearing
- General purpose I/O (GPIO) supporting 3.3V built-in CDR for SGMII, 1067 Mbps DDR3 and 1600 Mbps



### Features for Increased Reliability

- SEU-immune FPGA configuration cells
- Built-in SECEDED and memory interleaving on LSRAMs
- System controller suspend mode for safety-critical designs

### Security Features

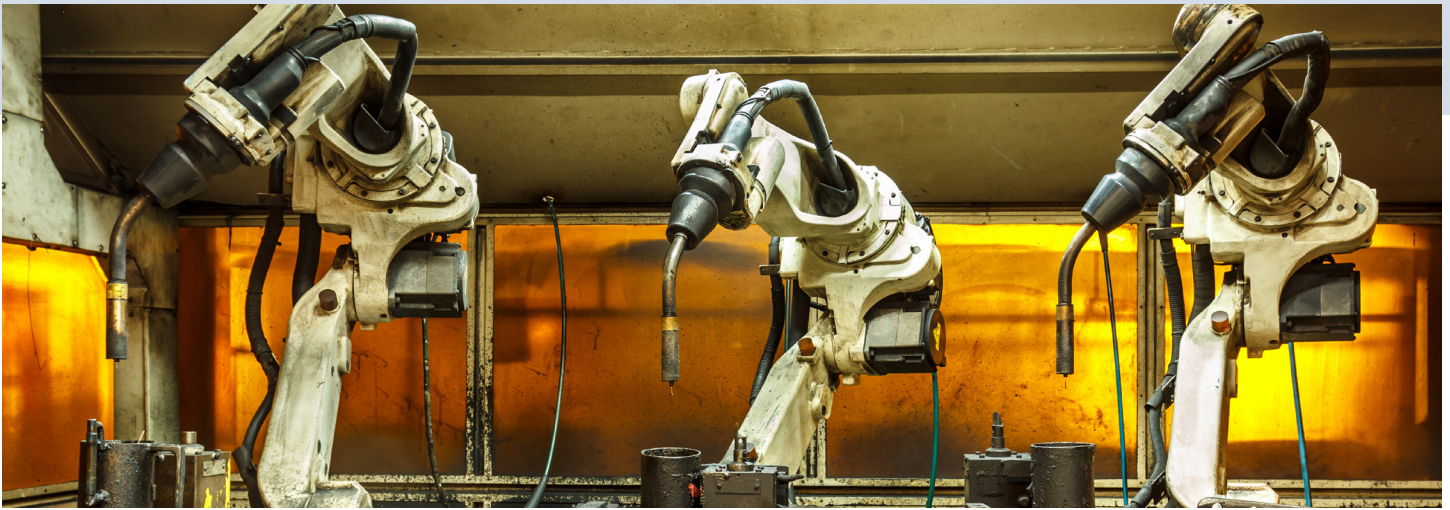
- Cryptography Research Incorporated (CRI)-patented, Differential Power Analysis (DPA)-safe bitstream protection.
- Integrated Physically Unclonable Function (PUF)
- 56 Kbytes of secure eNVM (sNVM)
- Built-in tamper detectors and countermeasures
- Integrated Athena TeraFire EXP5200B crypto co-processor
- Digest integrity check for FPGA, μPROM and sNVM
- True random number generator CRI DPA countermeasure pass-through license

## PolarFire FPGA Product Table

	Features	MPF050	MPF100	MPF200	MPF300	MPF500
<b>FPGA Fabric</b>	Logic Elements (4LUT + DFF)	48	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 kbit)	160	352	616	952	1520
	uSRAM Blocks (64 × 12)	460	1008	1764	2772	4440
	Total RAM (Mbits)	3.6 Mbits	7.6 Mbits	13.3 Mbits	20.6 Mbits	33 Mbits
	uPROM (kbits)	216 Kbits	297 Kbits	297 Kbits	459 Kbits	513 Kbits
	User DLLs/PLLs	8 each	8 each	8 each	8 each	8 each
<b>High-Speed I/O</b>	12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
<b>Total I/O</b>	Total User I/O	176	296	364	512	584
<b>Packaging</b>	<b>Type/Size/Pitch</b>	<b>Total User I/O (HSIO/GPIO) CDRs/XCVRs</b>				
<b>Extended Commercial/Industrial Grade</b>	FCSG325 (11 × 11, 11 × 14.5*, 0.5 mm)	164 (84/80) 6/4	170 (84/86) 7/4	170 (84/86) 7/4*		
	FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
	FCVG484 (19 × 19, 0.8 mm)	188 (96/92) 7/4	284 (120/164) 13/4	284 (120/164) 13/4	284 (120/164) 13/4	
	FCG484 (23 × 23, 1.0 mm)		244 (96/148) 12/8	244 (96/148) 12/8	244 (96/148) 12/8	
	FCG784 (29 × 29, 1.0 mm)			364 (132/232) 18/16	388 (156/232) 18/16	388 (156/232) 18/16
	FCG1152 (35 × 35, 1.0 mm)				512 (276/236) 19/16	584 (324/260) 19/24
<b>Military Grade ("S" Devices only)</b>	FCS325 (11 × 14.5, 0.5 mm)			170 (84/86) 7/4*		
	FCS536 (16 × 16, 0.5 mm)				300 (120/180) 15/4	
	FCV484 (19 × 19, 0.8 mm)				284 (120/164) 13/4	
	FC484 (23 × 23, 1.0 mm)				244 (96/148) 12/8	
	FC784 (29 × 29, 1.0 mm)				388 (156/232) 18/16	388 (156/232) 18/16
	FC1152 (35 × 35, 1.0 mm)					584 (324/260) 19/24
<b>Automotive T2 Grade</b>	FCSG325 (11 × 11, 11 × 14.5*, 0.5 mm)	164 (84/80) 6/4	170 (84/86) 7/4	170 (84/86) 7/4*		
	FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
	FCVG484 (19 × 19, 0.8 mm)	188 (96/92) 7/4	284 (120/164) 13/4	284 (120/164) 13/4	284 (120/164) 13/4	
	FCG484 (23 × 23, 1.0 mm)		244 (96/148) 12/8	244 (96/148) 12/8		
	FCG784 (29 × 29, 1.0 mm)					
	FCG1152 (35 × 35, 1.0 mm)					

Devices in the same package and family type are pin migratable

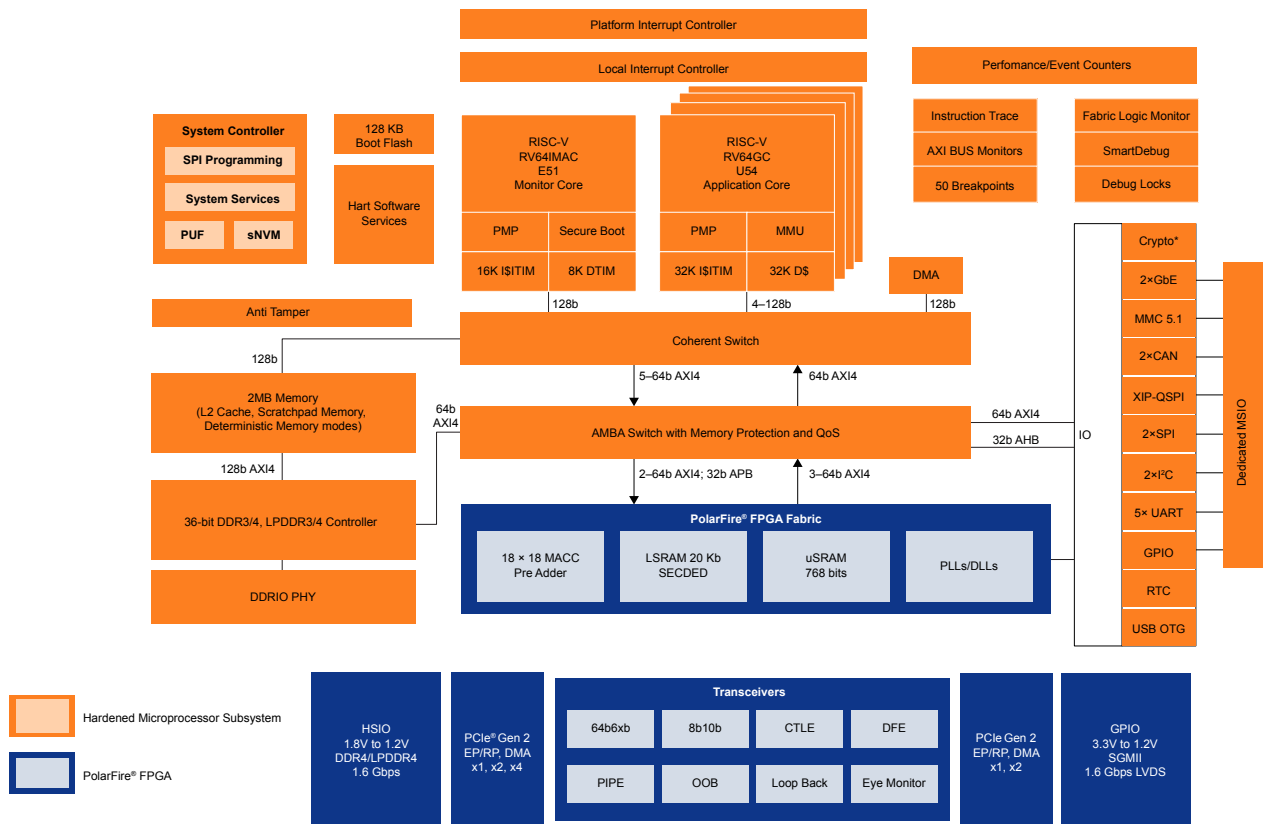
\*FCSG325 package has dimensions of 11 × 11 for MPF050 and MPF100 devices and 11 × 14.5 for MPF200 devices.



## PolarFire SoC FPGAs: Low-Power, Secure and Reliable Mid-Range SoC FPGA Platforms

Take advantage of the following features:

- Logic density of 23k to 461 kLEs
- Memory support: hard DDR controller and PHY for DDR4/LPDDR4, DDR3L and DDR3/LPDDR3
- Up to 20 12.7-Gbps SerDes ports
- Integrated dual PCIe for up to four Gen 2 Endpoint (EP) and Root Port (RP) designs
- Physically Unclonable Function (PUF)
- High-Speed I/O (HSIO) and LVDS up to 1600 Mbps
- Instant on, nonvolatile technology that offers 50% lower power compared to equivalent SRAM FPGAs
- All the security and reliability features of PolarFire FPGAs



## PolarFire FPGA Development Hardware

### PolarFire SoC FPGA Adds a Versatile, Low-Power Multi-Core RISC-V CPU Sub-System

- 64-bit multi-core CPU cluster coherent with the memory subsystem that enables Linux® and real-time operating systems in a deterministic AMP system
- Caches that are configurable as addressable memory
- Integrated DDR3/4, LPDDR3/4 controller and PHY
- Defense-grade secure boot
- Spectre and meltdown immune
- Physical memory protection
- SECDED on all memories
- Smallest form factors (11 × 11, 16 × 16 and 19 × 19)

### PolarFire SoC FPGA Product Table

	Features	MPFS025T	MPFS095T	MPFS160T	MPFS250T	MPFS460T
<b>FPGA Fabric</b>	K Logic Elements (4 LUT + DFF)	23	93	161	254	461
	Math Blocks (18 × 18 MACC)	68	292	498	784	1420
	LSRAM blocks (20 kbit)	84	308	520	812	1460
	µSRAM Blocks (64 × 12)	204	876	1494	2352	4260
	Total RAM (Mbits)	1.8	6.7	11.3	17.6	31.6
	µPROM (Kbits)	194	387	415	470	553
	User DLLs/PLLs	8 each	8 each	8 each	8 each	8 each
<b>High-Speed I/O</b>	250 Mbps to 12.5 Gbps SERDES lanes	4	4	8	16	20
	PCIe® Gen 2 endpoints/root ports	2	2	2	2	2
<b>Total FPGA I/O</b>	HSIO+GPIO	108	276	312	372	468
<b>Total MSS I/O</b>	MSS I/O	136	136	136	136	136
<b>MSS DDR DB</b>	MSS DDR Data Bus	16/32*	16/32*	32	32	32
<b>Packaging</b>	<b>Type/Size/Pitch (Commercial/Industrial)</b>	<b>MSS IO/HSIO/GPIO/XCVRs</b>				
<b>Extended Commercial/Industrial Grade</b>	FCSG325 (11 mm × 11 mm, 11 mm × 14.5 mm 4, 0.5 mm)*	102/32/48/2	102/32/48/2	—	—	—
	FCSG536 (16 mm × 16 mm, 0.5 mm)	—	136/60/108/4	136/60/108/4	136/60/108/4	—
	FCVG484 (19 mm × 19 mm, 0.8 mm)	136/60/48/4	136/60/84/4	136/60/84/4	136/60/84/4	—
	FCVG784 (23 mm × 23 mm, 0.8 mm)	—	136/144/132/4	136/144/168/8	136/144/180/8	—
	FCG1152 (35 mm × 35 mm, 1.0 mm)	—	—	—	136/144/228/16	136/180/288/20
<b>Military Grade ("S" devices only)</b>	<b>Type/Size/Pitch (Military)</b>					
	FCS325 (11 mm × 14.5 mm 4, 0.5 mm)	—	102/32/48/2	—	—	—
	FCS536 (16 mm × 16 mm, 0.5 mm)	—	—	—	136/60/108/4	—
	FCV484 (19 mm × 19 mm, 0.8 mm)	—	—	—	136/60/84/4	—
	FCV784 (23 mm × 23 mm, 0.8 mm)	—	—	—	136/144/180/8	—
	FC1152 (35 mm × 35 mm, 1.0 mm)	—	—	—	136/144/228/16	136/180/288/20
<b>Automotive T2 Grade</b>	<b>Type/Size/Pitch (Automotive)</b>					
	FCSG325 (11 mm × 11 mm, 11 mm × 14.5 mm 4, 0.5 mm)	102/32/48/2	102/32/48/2	—	—	—
	FCSG536 (16 mm × 16 mm, 0.5 mm)	—	136/60/108/4	136/60/108/4	136/60/108/4	—
	FCVG484 (19 mm × 19 mm, 0.8 mm)	136/60/48/4	136/60/84/4	136/60/84/4	136/60/84/4	—
	FCVG784 (23 mm × 23 mm, 0.8 mm)	—	136/144/132/4	136/144/168/8	136/144/180/8	—
	FCG1152 (35 mm × 35 mm, 1.0 mm)	—	—	—	—	—

Devices in the same package and family type are pin migratable

+ FCSG325 package has dimensions of 11×11 for MPFS025 and 11×14.5 for MPFS095 devices.

\* The MSS DDR bus is 16-bit wide in the FCSG325 package.

## Software and Tools

**Libero SoC Design Suite** offers high productivity with its comprehensive, easy to learn and adapt development tools for designing with Microchip's power efficient flash FPGAs, SoC FPGAs, and Rad-Tolerant FPGAs. It provides you with an efficient hardware design, easy to use, faster debug tool incorporating RTL entry through programming, a rich IP library, complete reference designs and development kits.

Benefit from:

- Best-in-class power, performance, and area optimizations
- Easy block-based system design
- Intuitive design flow
- Reduced debug time using our fast RTL to chip debug tools with minimal fabric resources.
- Accelerated design with Rich library of integrated IP cores

**Soft Console** offers comprehensive development and debugging assistance for Microchip SoC and non SoC based FPGAs. It facilitates:

- Efficient Embedded Software Design: Streamline software design and debugging processes through QEMU, allowing rapid iteration and testing
- Enhanced Debugging Capabilities: Support for both hard and soft RISC-V processors, early static code analysis, and industry standard GDB OpenOCD Debugging is provided
- Robust GIT Repository Integration: Leverage an extensive GIT repository for customizing open-source boot code, seamless integration of real-time and Linux-based sub-systems, and easy access to reference designs

**SmartHLS** converts software algorithms into hardware designs, speeding up development and optimizing FPGA's and SoC's implementations for faster time-to-market and efficient performance. The optimized HLS Open-Source libraries (Vision, Math, DSP, etc.) are available along with reference design only on GitHub, for public use and modifications.

**Math Library:** <https://github.com/MicrochipTech/fpga-hls-libraries/tree/main/math>

**Vision Library:** <https://github.com/MicrochipTech/fpga-hls-libraries/tree/main/vision>

The SmartHLS Compiler provides higher productivity as the designs have 2-5X faster development time, and debugging.

The performance is 2-10X higher compared to Embedded CPU, as the SmartHLS can offload computation to the fabric as well as use the embedded processor.

With SmartHLS one can:

- Design in C++ and verify the functionality with software tests
- Compile the C++ program into a functionality-equivalent Verilog hardware module
- Run co-simulation with ModelSim or QuestaSim to verify cycle-accurate hardware behavior and confirm that the hardware functionality matches the software

**IP Core Tools** help you accelerate your design productivity by providing an extensive suite of proven, optimized, and easy-to-use IP cores for use with Microchip FPGAs and SoC FPGAs. Libero SoC Design suite provides access to all the Microchip's inhouse IP Cores covering a broad range of functionality for example: Security, DSP, Motor Controller, Arithmetic etc. Moreover, Companion IP Cores are specialized IP cores that support targeted market requirements.

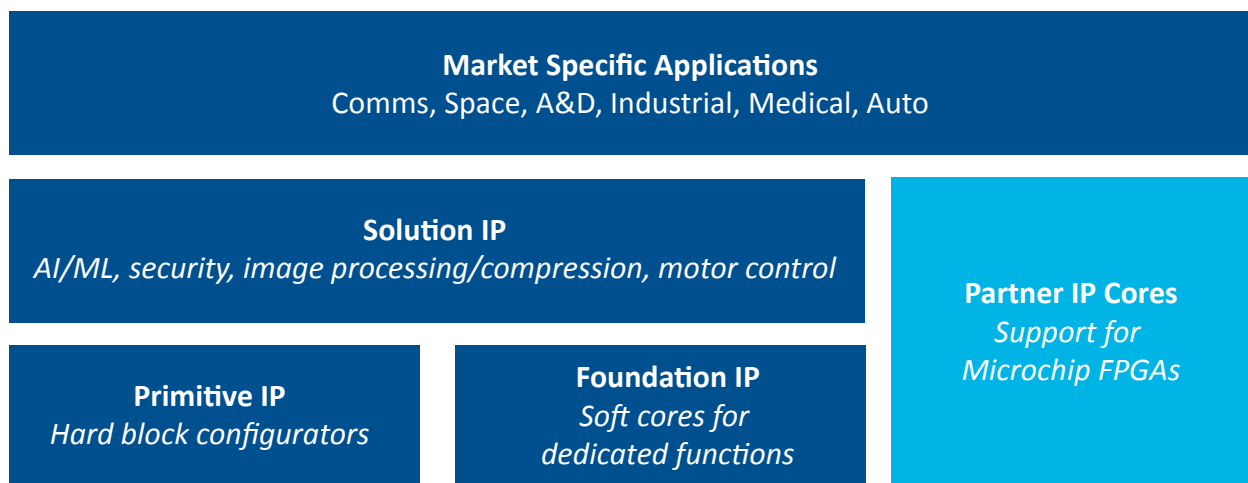


Figure: Microchip & Partner IP Cores serving various market segments

These IP Cores target various market segments like AI, ML, Aerospace and Defense and come with various licensing options as well available for purchase. With Microchip IP Core tools, you get:

- Fast IP integration using design environment, portable across FPGA families
- Accelerate hardware & software verification
- 200+ proven, optimized, and easy- to- use IP broad ecosystem of 120+ partner cores optimized for best area and timing
- Faster embedded software design

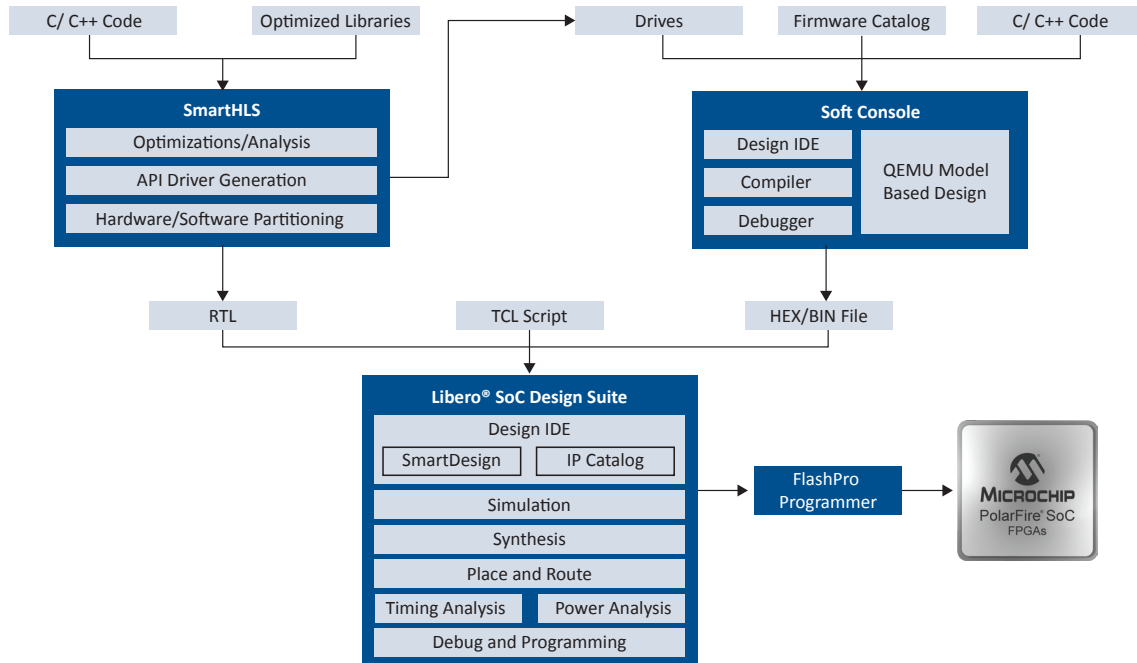
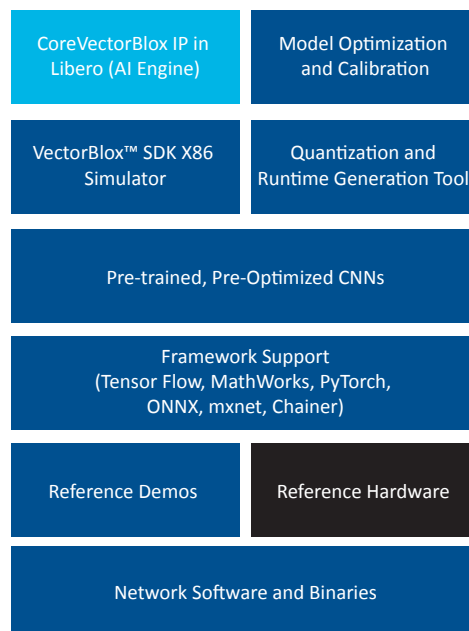


Figure: FPGA Software Design Flow

The VectorBlox™ Accelerator SDK is a Software Development Kit that offers the most power-efficient Convolutional Neural Network (CNN)-based Artificial Intelligence/Machine Learning (AI/ML) inference with PolarFire SoC and FPGAs. VectorBlox enables:

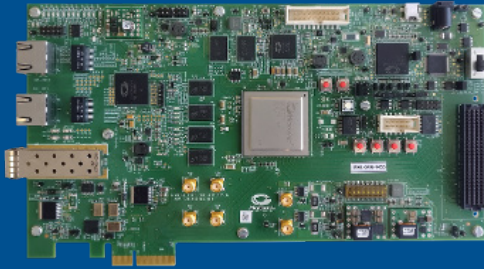
- OpenVINO™ toolkit-based front-end tools
- Support for most common frameworks like TensorFlow, Caffe, MxNet, PyTorch and DarkNet
- Quick evaluation without prior FPGA knowledge
- Software-overlay-based implementation; there is no need to reprogram the FPGA while updating CNNs



# PolarFire FPGA Development Hardware

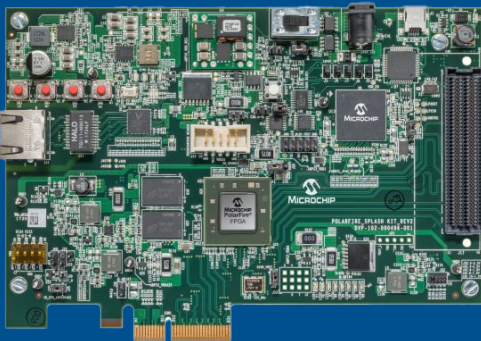
## PolarFire FPGA Evaluation Kit

MPF300-EVAL-KIT



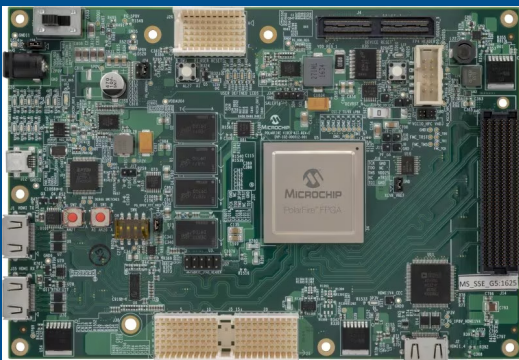
## PolarFire FPGA Splash Kit

MPF300-SPLASH-KIT



## PolarFire FPGA Video and Imaging Kit

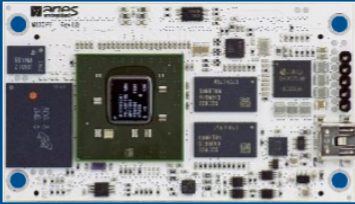
MPF300-VIDEO-KIT-NS



# PolarFire FPGA Development Hardware

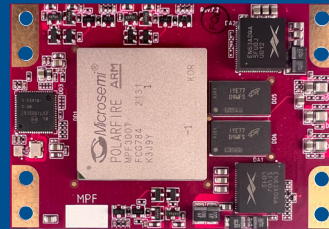
## Aries Embedded SoM

M100PF



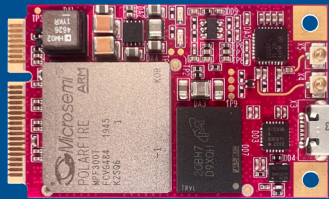
## Sundance DSP

SoM2- MPF300T



## Sundance Express SE 50.

SE50-MPF300T



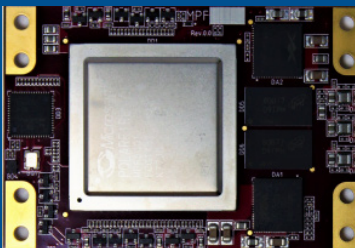
## Aldec

HES-MPF500-M2S150



## Sundance DSP

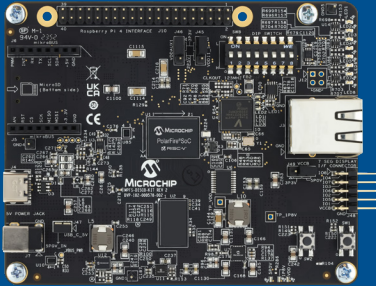
SoM1- MPF500T



# PolarFire SoC FPGA Development Hardware

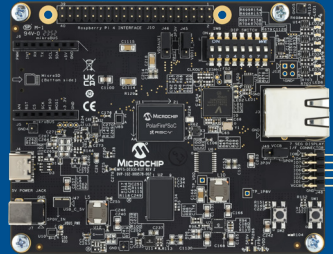
## PolarFire SoC Icicle Kit

MPFS-ICICLE-KIT-ES



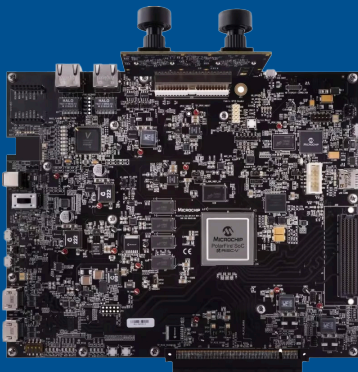
## PolarFire SoC Discovery Kit

MPFS-DISCO-KIT



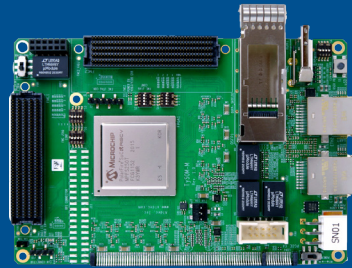
## PolarFire SoC Video Kit

MPFS250-VIDEO-KIT



## Aldec TySoM-M

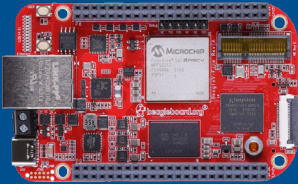
TySOM-M-MPFS250



# PolarFire SoC FPGA Development Hardware

## Beagleboard

BeagleV®-Fire



## Enktron KYNESIS SoM

KYNESIS – POLARFIRE RISC-V



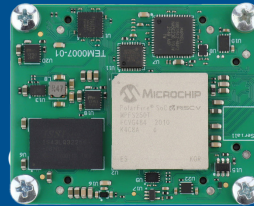
## Enclustra

Mercury+ MP1



## Trenz Electronic

TEM0007-01-CHE11-A



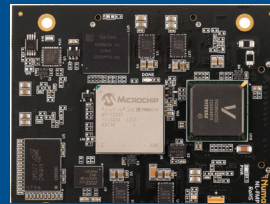
## Aries Embedded

M100PFS



## Numato Eagle Core SoM

NL-FMPS-B-001



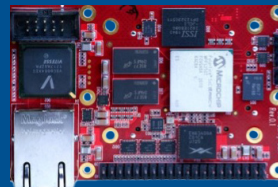
## Conclusive Engineering

RCHD-PF



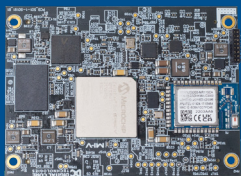
## Sundance Polarberry SoM

PB-MPFS250T-FCVG484E



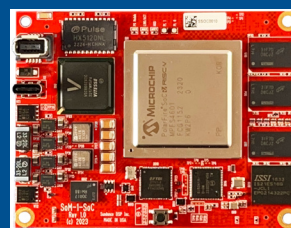
## Digitalcore Technologies

CMSV\_A1\_PF254\_AX



## Sundance DSP

SOM1-SOC





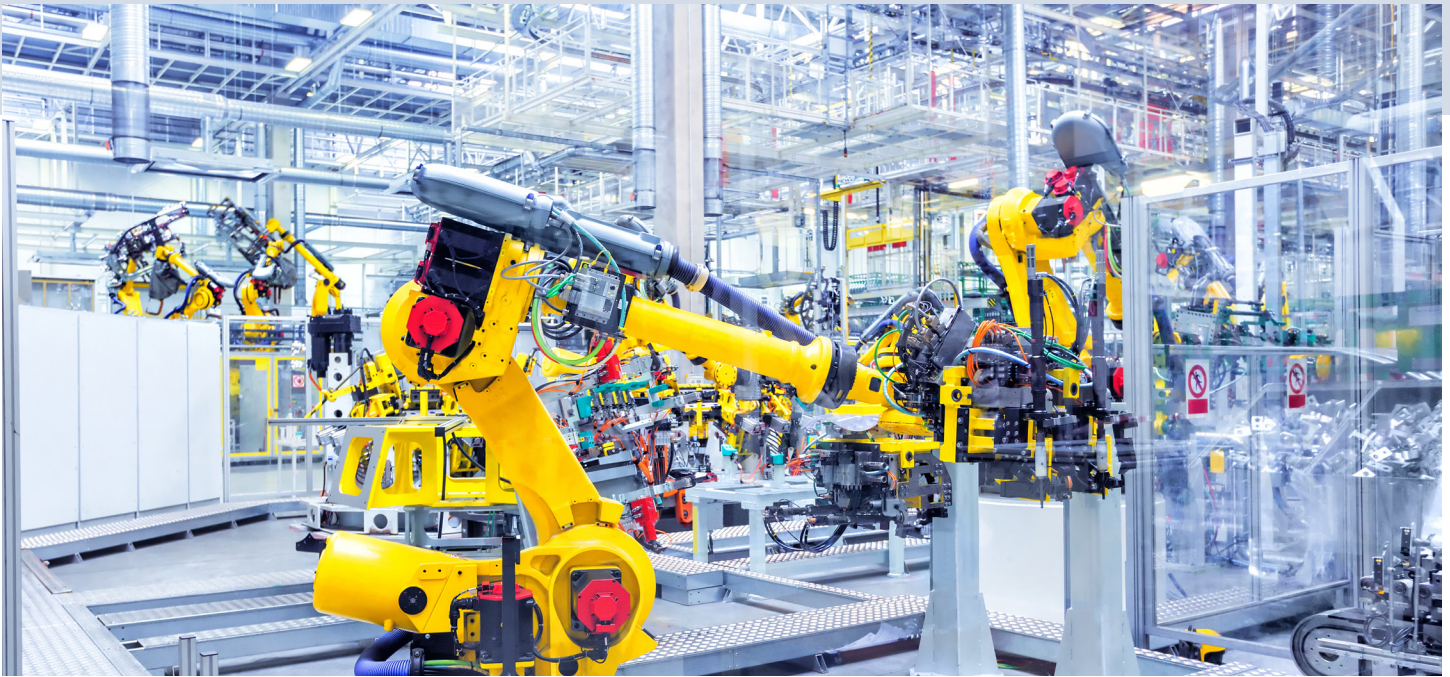
Mi-V, pronounced “my five,” is our continuously expanding, comprehensive suite of tools and design resources that we developed with numerous third parties to support RISC-V designs. The Mi-V ecosystem aims to increase adoption of the RISC-V Instruction Set Architecture (ISA) and our SoC FPGA and RISC-V soft CPU portfolio.

### Operating Systems and RTOS



### Development Tools





## Hardware and Design Services

























## Middleware and IP













## Online Reference and Support

### Online reference

RISC-V Innovation Unleashed Trainings



How-To YouTube Videos



Mi-V Virtual Summit Session Archive



Mi-V Ecosystem Unleashed Webinars



Renode Webinars



### Support

GitHub Discussions



Tech Support Portal



Microchip Technology Inc. | 2355 W. Chandler Blvd. | Chandler AZ, 85224-6199 | [microchip.com](https://microchip.com)