Mi-V RISC-V Ecosystem

Mi-V

MICROCHIP

microchip.com

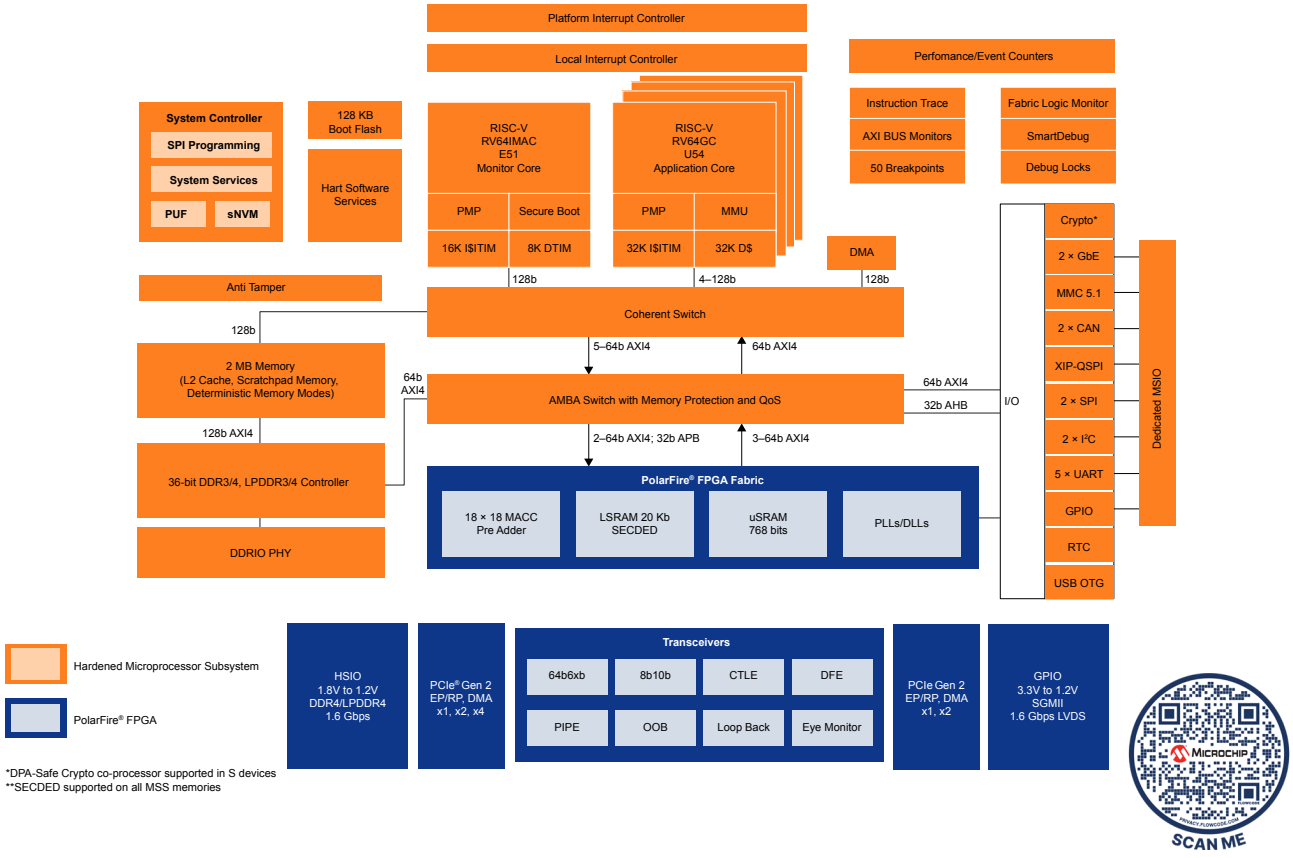
Mi-V (pronounced My-Five) is Microchip's initiative to influence the adoption of the RISC-V Instruction Set Architecture (ISA) with System-on-Chip (SoC) FPGAs and RISC-V based soft CPUs. The Mi-V ecosystem is a continuously expanding, comprehensive suite of tools and design resources developed by Microchip and numerous third parties to fully support RISC-V designs.

Mi-V Development Platforms

Our Mi-V ecosystem supports development using our RISC-V PolarFire® SoC FPGA and Mi-V Soft CPU platforms.

PolarFire SoC FPGA Platform:

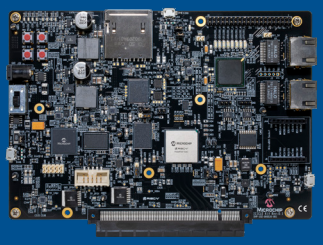
The PolarFire SoC FPGA family delivers a combination of power efficiency, thermal efficiency and defense-grade security for smart, connected systems. It is the first System-on-Chip (SoC) FPGA with a deterministic, coherent RISC-V CPU cluster and a deterministic L2 memory subsystem for creating Linux® and real-time applications. PolarFire SoC FPGAs offer from 25K to 460K Logic Elements (LEs) and feature 12.7 Gbps transceivers.



PolarFire SoC-Based System on Module (SoM) and Development Boards

PolarFire SoC Icicle Kit

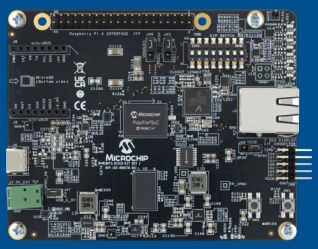
MPFS-ICICLE-KIT-ES



PolarFire SoC Video Kit

MPFS250-VIDEO-KIT

PolarFire SoC Discovery Kit

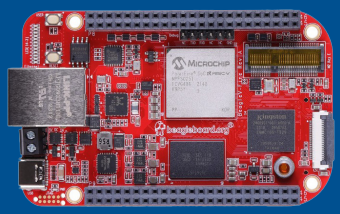


Aldec TySoM-M

Aries Embedded

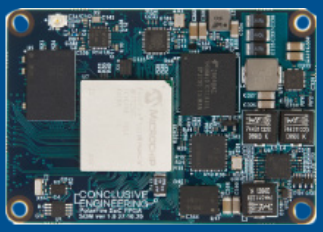
M100PFS

BeagleV®-Fire



Conclusive Engineering

RCHD-PF



Digitalcore Technologies

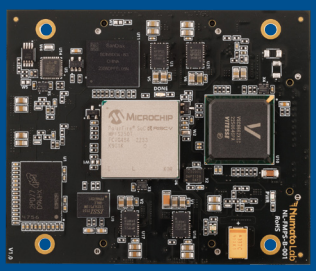
CMSV_A1_PF254_AX

Enclustra

Mercury+ MP1

Numato

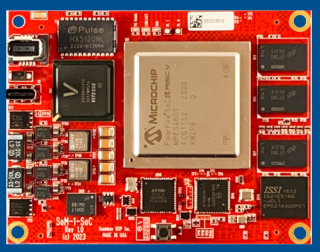
EagleCore PolarFire SoC SOM



Sundance DSP

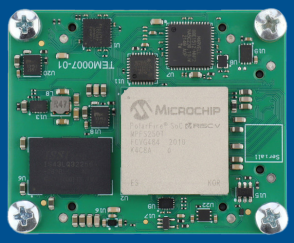
Polarberry

Sundance SoM1 SoC

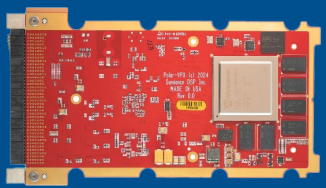


Trenz

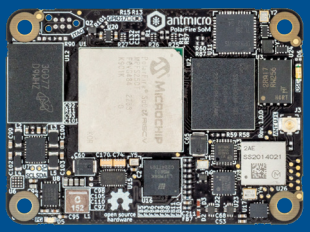
TEM0007-01-CHE11-A



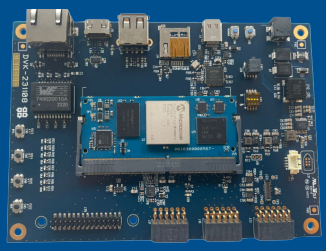
Sundance PolarVPX



Antmicro's Open Source PFSoC SoM



Enktron - Kynesis SoM



Mi-V Soft CPUs Portfolio:

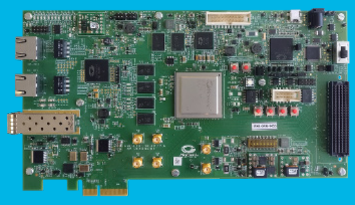
We offer a comprehensive RISC-V soft IP portfolio for FPGA designs. Mi-V RV32 soft CPUs are available for PolarFire SoC, PolarFire, RTG4™, and IGLOO® 2 FPGAs with complete design support through Libero® SoC Design Suite. The Eclipse-based SoftConsole IDE provides the embedded firmware development environment, a Renode emulation platform, a GCC compiler and the debuggers needed for C/C++ firmware development. Libero SoC Design Suite and the SoftConsole development environment provide all the required tools to integrate Mi-V soft CPUs in our FPGAs and develop, test and debug embedded firmware.

Portfolio

RISC-V	Mi-V RV32	Mi-V RV32IMAF_L1_AHB	Mi-V RV32IMA_L1_AHB	Mi-V RV32IMA_L1_AXI
LEs	4k–20k*	26k	10k	10k
CoreMark® Score	0.18–2.48	2.01	2.01	2.01
Cache Size	1 KB I$	2 KB I$, 8 KB D$	2 KB I$, 8 KB D$	2 KB I$, 8 KB D$
Trace	Optional**	N/A	N/A	N/A
Floating Point	Optional Single-Precision	Single-Precision	N/A	N/A

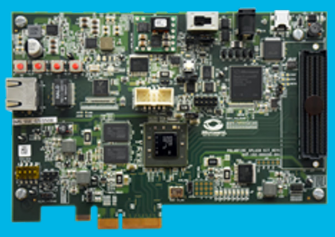
*The Mi-V RV32 is recommended for all new designs
**Raw Trace requires additional Trace Encoder IP

PolarFire Evaluation Kit

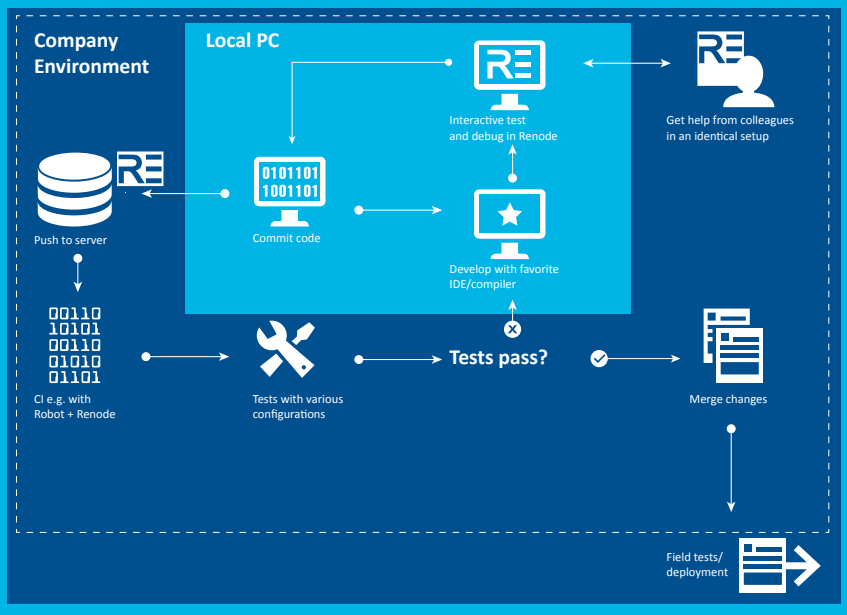


Mi-V Creative Board

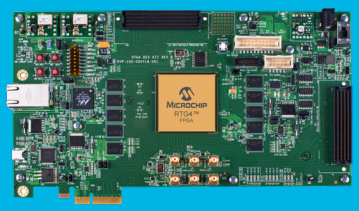
Splash Kit



Renode



RTG4™ FPGA Development Kit



SCAN ME

Online References and Support

Online References

RISC-V Innovation Unleashed Trainings

How-To YouTube Videos

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Mi-V Virtual Summit Session Archive

Mi-V Ecosystem Unleashed Webinars

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Renode Webinars

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Support

GitHub Discussions

Technical Support Portal

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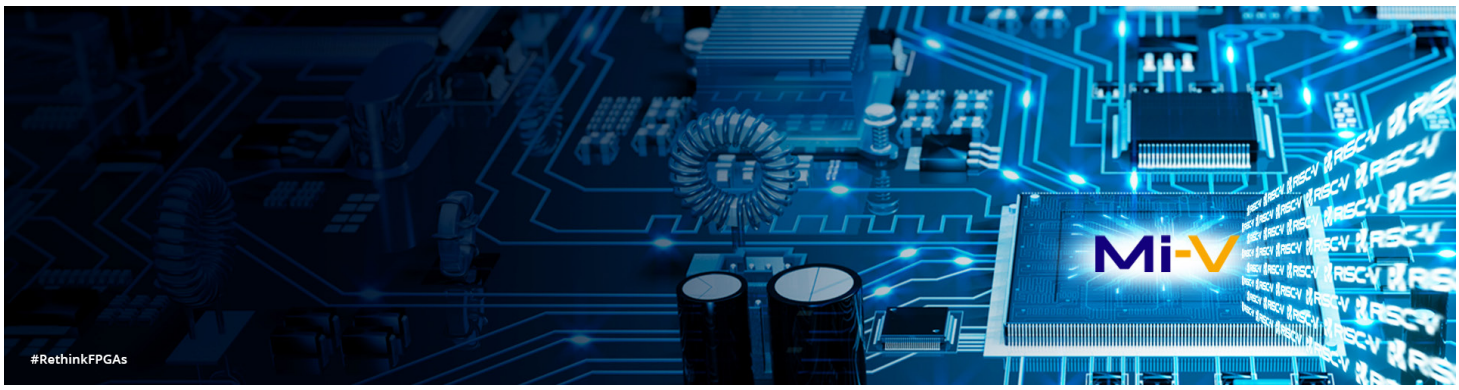

Operating Systems and RTOS

yocto PROJECT
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RIOT
freeRTOS
Zephyr
seL4 FOUNDATION
NUCLEUS
µ-velOSity
INTEGRITY
SIEMENS
WNDRVR
SAFERTOS highintegritysystems WITTENSTEIN
SYSGO EMBEDDING INNOVATIONS
Microsoft Azure
ROS
RTEMS
MontaVista
VxWorks
eCosCentric
SUSE
oce TECHNOLOGY
LynxOS FROM LYNUXWORKS

Development Tools

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Libero System-on-Chip
iar
Green Hills SOFTWARE
SEGGER
SIEMENS
ASHLING
TASKING
SoftConsole
LDRA
MathWorks
VECTOR
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Middleware and IP

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