

## Metastability Characterization Report for FPGAs [\(Ask a Question\)](#)

Whenever asynchronous data is registered by a clocked flip-flop, there is a probability of a setup or hold time violation on that flip-flop. In applications such as synchronization or data recovery, due to the asynchronous nature of the data input to the flip-flops, the data transition time is unpredictable with respect to the active edge of the clock. The susceptibility of a circuit to reach a metastable state can be described using a probabilistic equation. Setup or hold violations cause the output of the flip-flop to enter a symmetrically balanced transient state, called a metastable state.

The metastable state is manifested in a bistable device by the outputs glitching, entering an undefined state somewhere between a "1" and "0," oscillating, or by a delayed output transition for an indeterminable amount of time. Once the flip-flop has entered the metastable state, the probability that it will still be metastable later has been shown to be an exponentially decreasing function of time. Because of this property, a designer should simply wait for an additional time after the specified propagation delay before sampling the flip-flop output so that the designer can be assured that the likelihood of metastable failure is remote enough to be tolerable. The additional time of waiting becomes shorter, even though still greater than zero, as technology improves and semiconductor devices reach higher speeds.

This document describes the metastability equations, followed by the metastability characterization of Microchip RTG4™, PolarFire® and RT PolarFire FPGAs and SoCs. This application note also provides an example on the usage of the metastability equations.

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## 1. Theory of Metastability (Ask a Question)

In general, the Mean Time Between Failures (MTBF) should be defined statistically. The following figure illustrates a simple circuit used to synchronize asynchronous data with the system clock. EQ1 shows the relation between MTBF and the clock-to-out settling time of a flip-flop:

**Equation 1-1.** EQ1

$$MTBF = \left( e^{\left( \frac{T_S}{\tau} \right)} \right) / (T_0 \cdot f_d \cdot f_c)$$

**Equation 1-2.** EQ2

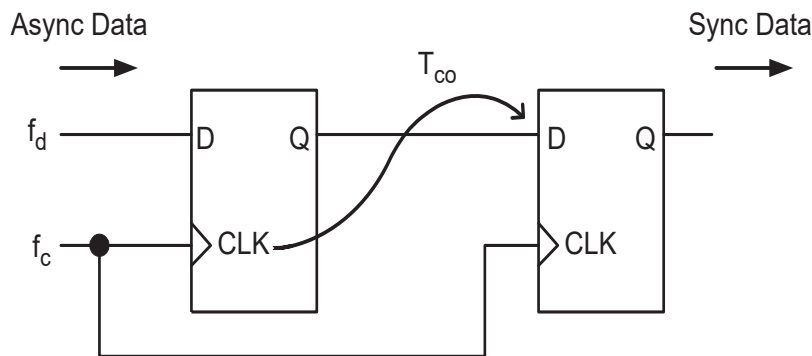
$$T_S = T_{co} + T_{met}$$

The following is a list of parameters in the preceding equations:

- $T_S$  = Total flip-flop output settling time.
- $T_{co}$  = Flip-flop clock-to-out delay.
- $T_{met}$  = Additional settling time added to the normal clock-to-out delay of the flip-flop before sampling the output of the flip-flop.
- $\tau$  = Metastable decay constant.
- $T_0$  = Metastability aperture at  $T_{co} = 0$  ns (This parameter represents the likelihood that a flip-flop enters a metastable state).
- $f_d$  = Data transition rate (Twice the data frequency for periodic signals, as there are two transitions per one period).
- $f_c$  = Clock frequency

The following figure shows an example of synchronization circuit.

**Figure 1-1.** Example of Synchronization Circuit



The aperture indicates the likelihood of a flip-flop entering a metastable state. It is defined as a time window within the clock period. When data transitions occur within this aperture, the flip-flop's output settling time will exceed  $T_{co} + T_{met}$ . The aperture is calculated by counting the number of instances where the settling time exceeds the specified  $T_{co} + T_{met}$ . The metastability aperture decreases exponentially as the allowed settling time ( $T_{co} + T_{met}$ ) increases:

**Equation 1-3.** EQ3

$$Aperture = T_0 \cdot \left( e^{-((T_{co} + T_{met})/\tau)} \right)$$

If a data transition occurs within the aperture, the flip-flop will remain metastable beyond the allocated settling time ( $T_{co} + T_{met}$ ), causing the subsequent flip-flop to register invalid data. The probability of an asynchronous data transition is uniformly distributed over the clock period. Therefore, the probability of a single data transition occurring within the metastable aperture is calculated as per the following equation:

**Equation 1-4. EQ4**

$$p = (\text{aperture})/T_c$$

Where  $T_c$  is the clock period.

In each clock cycle, a failure occurs if the data transition time occurs within the aperture. Therefore, the number of failures per clock cycle can be derived from using the following equation:

**Equation 1-5. EQ5**

$$n_e = n \cdot p = (n \cdot (\text{aperture})/T_c)$$

Where  $n_e$  represents the number of errors per clock cycle, and  $n$  is the number of data transitions per clock period ( $f_d / f_c$ ).

The number of clock cycles in the operation time ( $N$ ) is the total time divided by the clock period:

**Equation 1-6. EQ6**

$$N = T_{operation}/T_c$$

Combining EQ5 and EQ6 results in the total number of failures per operation time ( $N_e$ ):

**Equation 1-7. EQ7**

$$N_e = N \cdot n_e = \left( (T_{operation}/T_c) \cdot ((f_d/f_c) \cdot ((\text{aperture})/T_c)) \right)$$

Since  $T_c = 1/f_c$ , EQ7 can be simplified to the following equation:

**Equation 1-8. EQ8**

$$N_e = T_{operation} \cdot f_d \cdot f_c \cdot \text{aperture}$$

MTBF is defined as the operation time divided by the number of failures:

**Equation 1-9. EQ9**

$$MTBF = 1/(f_d \cdot f_c \cdot \text{aperture}) = 1/(T_0 \cdot e^{-(T_{co} + T_{met})/\tau} \cdot f_d \cdot f_c)$$

## 2. FPGA Metastability Characterization [\(Ask a Question\)](#)

Like other FPGA manufacturers, to absorb the fixed value of the  $e^{T_{CO}}$  term, Microchip simplifies [EQ9](#) to the following form:

**Equation 2-1.** EQ10

$$MTBF = e^{(C2 \cdot T_{met})} / (C1 \cdot fd \cdot fc)$$

Where C2 is a constant inversely proportional to the metastability decay constant, and C1 is the proportionality constant that is similar to aperture.

The FPGA metastability characterization is a series of tests that are conducted in order to identify the values of C1 and C2. There are several environmental and test condition factors that influence the characterization. These factors include but are not limited to the rise time of data and clock signals, input voltage levels and operating voltage and temperature. Moreover, increased system noise due to switching of both internal nodes and I/Os can influence the metastability results. Therefore, it is essential to provide a suitable environment for testing.

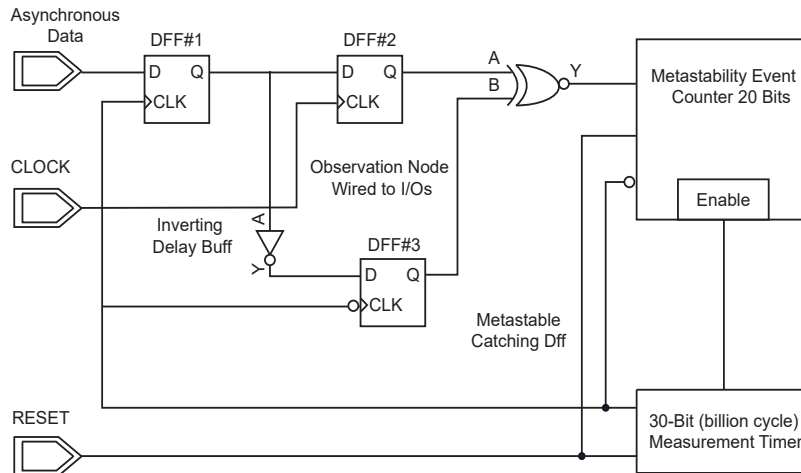
### 3. Test Design Description [\(Ask a Question\)](#)

The following figure shows a schematic of the test circuit used to characterize the metastability in Microchip devices. The propagation delay, operating under specified setup and hold time, is measured from the output of flip-flop DFF#1 to the input of flip-flop DFF#3. This value is denoted by:

**Equation 3-1.** EQ11

$$T_{\min} = T_{\text{cof}}(\text{DFF1}) + T_{\text{delay}} + T_{\text{su}}(\text{DFF3})$$

**Figure 3-1.** Test Circuit



In this design, several timing parameters are crucial for characterizing metastability.  $T_{\text{delay}}$  is the propagation delay from output of DFF#1 to the input of DFF#3.  $T_{\text{cof}}$  is the clock-to-out delay of DFF#3, and  $T_{\text{su}}$  represents the setup time requirement of DFF#3.  $T_{\min}$  corresponds to the  $T_{\text{co}}$  in [Equation 1-9](#) and is the reference time to which the additional settling time,  $T_{\text{metr}}$  is added for metastability characterization.

DFF#2 is clocked on the same edge as DFF#1, while DFF#3 must resolve the signal driven from the metastable DFF#1 before the falling clock edge. As shown in the preceding figure, the interval  $T_{\min} + T_{\text{metr}}$  which is the time between the clock's rising and falling edges, can be easily set or measured by adjusting the duty cycle of the clock signal. A detectable metastable event occurs when DFF#2 and DFF#3 are in the same state. In the expected operation, DFF#2 and DFF#3 are in opposite states due to the inverter in the DFF#3 input data path. The XNOR gate allows the event counter to record these metastable events. After a billion clock cycles, the counter is read and the MTBF is calculated. In this test,  $T_{\min}$  was determined with a precision of  $\pm 0.01\%$  of the duty cycle at 10 MHz, corresponding to an error margin of  $\pm 10$  ps.

The following is a list of other test setup parameters:

- Clock and data inputs are driven from independent pulse generators (<1 ns rise time)
- The clock input levels range from 0V to 2.5V. These levels were required due to impedance matching requirements of our test fixture. Data input is driven from 0V to 2.5V.
- RTG4™ power supply settings are as follows:
  - VDD at 1.2V
  - VPP at 2.5V
  - VDDI at 2.5V
- PolarFire® power supply settings are as follows:

- VDD tested at both 1.0V and 1.05V modes
- VDDA tested at both 1.0V and 1.05V modes
- VDDA<sub>25</sub> at 2.5V
- VDD<sub>25</sub> at 2.5V
- VDDI at 2.5V
- VDD\_XCVR\_CLK at 2.5V

## 4. Metastability Measurement Results [\(Ask a Question\)](#)

EQ10 can be reformed into the following equation:

**Equation 4-1.** EQ12

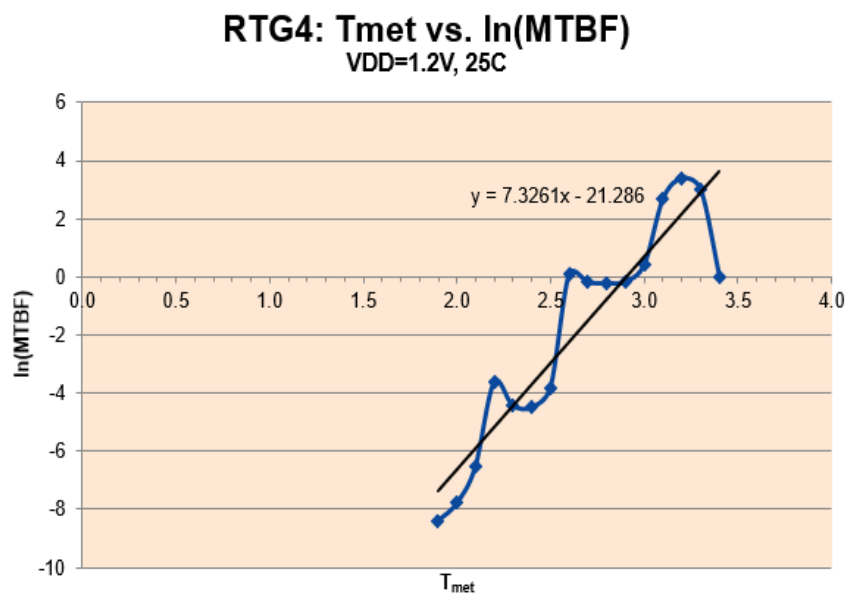
$$\ln(MTBF) = C2 \cdot T_{met} - \ln(C1 \cdot f_d \cdot f_c)$$

The plot of the preceding equation is a linear relationship between  $\ln(MTBF)$  and  $T_{met}$ , where  $C2$  is the slope of the line.

### 4.1. Metastability Measurement Results for RTG4 [\(Ask a Question\)](#)

The following figure shows the plot of EQ12 for Microchip RTG4™ family.  $C1$  and  $C2$  can be calculated from any two data points.

**Figure 4-1.** RTG4 Metastability Plot



The metastability theory indicates that  $C1$  and  $C2$  are independent of the test clock and data frequency. The test results concur within experimental tolerances. The calculation of  $C1$  and  $C2$  is listed in the following table.

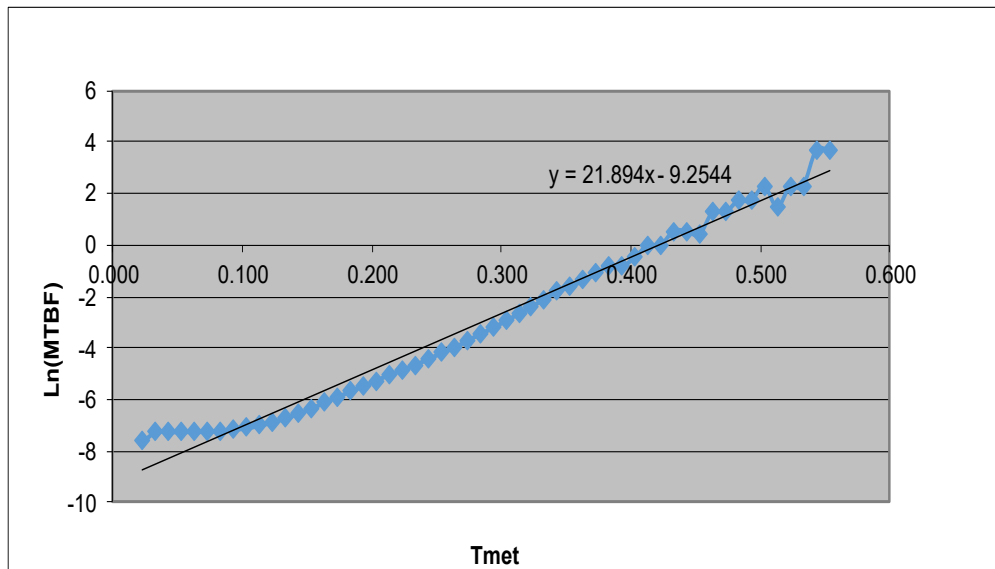
**Table 4-1.** RTG4 Metastability Data

M	B	C1	C2
7.33	-21.29	2.877E-05	7.326E+09

### 4.2. Metastability Measurement Result for PolarFire Family [\(Ask a Question\)](#)

The following figure shows the plot of Metastability for Microchip PolarFire® family, including PolarFire, PolarFire SoC, RT PolarFire and RT PolarFire SoC.  $C1$  and  $C2$  can be calculated from any two data points.

Figure 4-2. PolarFire Metastability Plot



The test results concur within experimental tolerances. The calculation of C1 and C2 is listed in the following table.

Table 4-2. PolarFire Metastability Data

M (Hz)	B (Constant)	C1 (s)	C2 (Hz)
21.894	-9.2544	2.45E-11	2.1894E+10



**Important:** Where,

- M – Slope of  $\ln(\text{MTBF})$  vs.  $T_{\text{met}}$  (in per nano seconds)
- B – Intercept of  $\ln(\text{MTBF})$  vs.  $T_{\text{met}}$
- C1 – Proportionality constant from B
- C2 – Proportionality constant from M

## 5. Examples of Metastability Coefficients Usage [\(Ask a Question\)](#)

This section provides the examples of metastability coefficients usage for the RTG4™ and PolarFire® Family of FPGA and SoC devices.

### 5.1. RTG4 Examples [\(Ask a Question\)](#)

Metastability is statistical nature, and designers should allow enough additional time ( $T_{met}$ ) to ensure the likelihood of metastable failure is remote enough to meet the design specifications.

For example, consider the simple circuit in [Figure 1-1](#), implemented on an RTG4 device to synchronize an asynchronous data input to the FPGA. The design parameters provided, either through design specification or post-layout timing analysis, are as follows:

- System clock rate ( $f_c$ ): 100 MHz to capture the asynchronous events.
- Asynchronous data transition rate = 12.5 MHz
- Tolerable MTBF = 20 years

If the designer does not allow additional sampling time ( $T_{met} = 0$ ) and operates the clock at the rate of 100 MHz, the resulting MTBF is calculated as 27.81 ps using [EQ10](#). This means a metastability error would occur at the second flip-flop output every 27.81 ps—far exceeding the required MTBF of 20 years indicated in the design specification. To meet this requirement, the designer must allow additional  $T_{met}$  in the settling time, which can be calculated using the following approach:

1. Convert 20 years to seconds:  $20 \text{ years} = 20 * 365 * 24 * 3600 = 630,720,000 \text{ seconds}$
2. Solve for  $T_{met}$  using the MTBF formula in [EQ12](#):  $\ln(630,720,000) = 7.326E+09 * T_{met} - \ln(2.877E-05 * 100E6 * 12.5E6)$  results in  $T_{met} = 6.08 \text{ ns}$ .

Thus, an additional 6.08 ns of settling time satisfies the required MTBF.

According to the [DS0131: RTG4 FPGA Datasheet](#), when using the SET filter on the fabric flip-flops (FF), the worst-case clock-to-Q,  $T_{CLKQ}$  is 0.243 ns, and the worst-case data setup time,  $T_{SUD}$  is 1.3 ns. For the 2-FF synchronizer circuit shown in [Figure 1-1](#), assume the worst-case  $T_{CO} = T_{CLKQ} + T_{SUD} = 1.543 \text{ ns}$  with SET filter enabled. Without SET filter enabled, the worst-case  $T_{SUD}$  is 0.505 ns, implying a  $T_{CO} = 0.748 \text{ ns}$ .

This implies that the circuit in [Figure 1-1](#) has a max achievable settling time equal to  $T_c$  (clock period) -  $T_{CO}$ :

- **With SET filter:** Max  $T_{met}$  achievable is  $10 \text{ ns} - 1.543 \text{ ns} = 8.45 \text{ ns}$ .
- **Without SET filter:** Max  $T_{met}$  achievable is  $10 \text{ ns} - 0.748 \text{ ns} = 9.25 \text{ ns}$ .

Thus, the 2-FF synchronizer meets the required 6.08 ns of additional settling time in this design example.

As another example, consider if the clock rate used in the previous example was increased to 160 MHz:

1. Calculate  $T_{met}$  as follows:

$$\ln(630,720,000) = 7.326E+09 * T_{met} - \ln(2.877E-05 * 160E6 * 12.5E6)$$

Resulting in  $T_{met} = 6.15 \text{ ns}$

Thus, with  $f_c = 160 \text{ MHz}$ , an additional 6.15 ns of settling time will fulfill the required MTBF.

2. Determine max achievable  $T_{met}$  for the 2-FF synchronizer, considering the smaller clock period:
  - **With SET filter:** Max  $T_{met} = 6.25 \text{ ns} - 1.543 \text{ ns} = 4.70 \text{ ns}$ .
  - **Without SET filter:** Max  $T_{met} = 6.25 \text{ ns} - 0.748 \text{ ns} = 5.50 \text{ ns}$ .

The designer must consider that the 2-FF synchronizer circuit shown in [Figure 1-1](#) would not allow sufficient settling time to reliably capture the asynchronous input signal. A third FF stage could be added to the synchronizer to allow additional settling time before the asynchronous signal is sampled by the rest of the user design. To generalize for RTG4, when the design clock frequency exceeds 125 MHz, it is recommended to increase the number of synchronizer flip-flops used beyond the typical 2-FF design shown in [Figure 1-1](#).

In general, another point to consider is the total number of such synchronizer circuits used in the design. The overall MTBF of the entire design decreases as the number of these synchronizer circuits used increases. For example, if a 20 year MTBF is used in the calculations above for 1 synchronizer instance, then a 200 year MTBF can be entered in the formula for a design containing 10 such synchronizer instances to still meet the 20 year goal for the entire design.

## 5.2. PolarFire Examples (Ask a Question)

Consider the circuit shown in [Figure 1-1](#) being used in the FPGA fabric of any device from the PolarFire® family to synchronize data from one clock domain to another clock domain.

For this example, the destination clock domain operates at a frequency ( $f_c$ ) of 160 MHz, while the incoming data transition rate is 80 MHz and tolerable MTBF is 20 years. However, if the designer does not allow additional settling time ( $T_{met} = 0$ ) before sampling the data, the MTBF, as calculated by [EQ10](#) will be 3.19  $\mu$ s. This indicates that the synchronizer circuit could experience a metastable output every 3.19  $\mu$ s, which does not meet the 20-year goal. The calculation with  $T_{met} = 0$  is as follows:  $MTBF = e^{(C2*0)} / (C1*fd*fc) = 1 / (2.45E-11 * 80,000,000 * 160,000,000) = 3.19 \mu s$ .

To meet the MTBF goal, the circuit design must allow additional  $T_{met}$  settling time before sampling the data. This can be calculated using the following approach:

1. Convert the MTBF goal to seconds:  $20 \text{ years} = 20 * 365 * 24 * 3600 = 630,720,000$  seconds
2. Solve [EQ12](#) for  $T_{met}$ :
  - $\ln(630,720,000) = 2.1894E+10 * T_{met} - \ln(2.45E-11 * 80E6 * 160E6)$
  - $T_{met} = 1.50 \text{ ns}$

Thus, an additional 1.50 ns of settling time satisfies the required MTBF for this synchronizer circuit.

The next step is to verify whether the 2-FF synchronizer circuit can achieve the required 1.50 ns settling time, based on the device's worst-case  $T_{CO}$  and the design parameters, such as clock period. The  $T_{CO}$  in this circuit depends on the flip-flop (FF)  $T_{clk2q} + T_{sud}$  when the two FFs are placed adjacent to each other. If they are placed apart, an additional routing delay  $T_{routing}$  is included. To maximize the achievable settling time provided by the 2-FF synchronizer circuit, minimizing the  $T_{CO}$  is crucial, therefore, placing the 2 flip-flops close together is recommended.



**Important:** For Clock Domain Crossing (CDC) synchronizer circuits between two clock domains, such as those referenced in [Figure 1-1](#), the Libero® SoC Design Suite default settings for PolarFire design **Synthesis and Compile** enables the identification of these circuits and attempt to place the synchronizer FFs close together.

For the PolarFire family of devices, the following is a list of FPGA fabric worst-case timing parameters for  $T_{clk2qFF} + T_{sudFF}$ :

- At 0 KRAD Radiation Exposure setting:  $T_{clk2qFF} + T_{sudFF} = 0.265 \text{ ns}$
- At 100 KRAD Radiation Exposure setting:  $T_{clk2qFF} + T_{sudFF} = 0.270 \text{ ns}$

This implies that the circuit in [Figure 1-1](#) has a maximum achievable settling time equal to the clock period  $T_c - T_{CO}$ :

- At 0 KRAD Radiation Exposure: Max  $T_{\text{met}}$  achievable is  $6.25 \text{ ns} - 0.265 \text{ ns} = 5.985 \text{ ns}$
- At 100 KRAD Radiation Exposure: Max  $T_{\text{met}}$  achievable is  $6.25 \text{ ns} - 0.270 \text{ ns} = 5.98 \text{ ns}$

Therefore, the 2-FF synchronizer meets the required 1.50 ns of additional settling time using the design parameters in this example.

If we consider the same example but change the  $f_c$  from 160 MHz to 320 MHz, the 2-FF synchronizer circuit analysis would indicate the following impacts:

- $T_{\text{met}} = 1.54 \text{ ns}$  of additional settling time required.
- At 0 KRAD Radiation Exposure: Max  $T_{\text{met}}$  achievable is  $3.125 \text{ ns} - 0.265 \text{ ns} = 2.86 \text{ ns}$
- At 100 KRAD Radiation Exposure: Max  $T_{\text{met}}$  achievable is  $3.125 \text{ ns} - 0.270 \text{ ns} = 2.855 \text{ ns}$

Therefore, the 2-FF synchronizer operating at 320 MHz would still meet the required 1.54 ns of additional settling time to meet the desired MTBF in this example.

## 6. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 6-1.** Revision History

Revision	Date	Description
A	11/2025	The following is a summary of the changes made in revision A of this document: <ul style="list-style-type: none"> <li>• The document was migrated from Microsemi template to Microchip template.</li> <li>• The document number was changed to DS00006287 from AC474.</li> <li>• Updated document to include Metastability Characterization results for PolarFire® Family of FPGAs and SoCs, in addition to the original RTG4™ results.</li> </ul>
1.0	06/2018	First publication of the document.

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