Metastability Characterization Report for Microsemi Flash FPGAs

Introduction

Whenever asynchronous data is registered by a clocked flip-flop, there is a probability of setup or hold time violation on that flip-flop. In applications such as synchronization or data recovery, due to the asynchronous nature of the data input to the flip-flops, the data transition time is unpredictable with respect to the active edge of the clock. The susceptibility of a circuit to reaching this metastable state can be described using a probabilistic equation. Setup or hold violations cause the output of the flip-flop to enter a symmetrically balanced transient state, called a metastable state. The metastable state is manifested in a bistable device by the outputs glitching, going into an undefined state somewhere between 1 and 0, oscillating, or by the output transition being delayed for an indeterminable time. Once the flip-flop has entered the metastable state, the probability that it will still be metastable later has been shown to be an exponentially decreasing function of time. Because of this property, a designer should simply wait for additional time after the specified propagation delay before sampling the flip-flop output so that the designer can be assured that the likelihood of metastable failure is remote enough to be tolerable. The additional time of waiting becomes shorter, even though still more than zero, as the technology improves and semiconductor devices reach higher ranges of speed.

This document discusses a description of metastability equations followed by metastability characterization of ProASIC,® ProASIC PLUS®, ProASIC3, and ProASIC3E FPGAs. This application note also provides examples on the usage of metastability equations.

Theory of Metastability

In general, the mean time between failures (MTBF) should be defined statically. Figure 1 on page 412 depicts a simple circuit, used to synchronize asynchronous data with the system clock. EQ 1 shows the relation between MTBF and the clock-to-out settling time of a flip-flop:

$$MTBF = e^{(Ts / \tau)} / (T_o \times f_d \times f_c)$$

EQ 1

$$T_s = T_{co} + T_{met}$$

EQ 2

In EQ 1 and EQ 2:

- T_s = Total flip-flop output settling time
- T_{co} = Flip-flop clock-to-out delay
- T_{met} = Additional settling time added to the normal clock-to-out delay of the flip-flop before sampling the output of the flip-flop
- t = Metastable decay constant.
- T_0 = Metastability aperture at T_{co} = 0 ns (this parameter represents the likelihood that a flip-flop will enter a metastable state)
- f_d = Data transition rate (twice the data frequency for periodic signals, since there are two transitions per period)
- f_c = Clock frequency

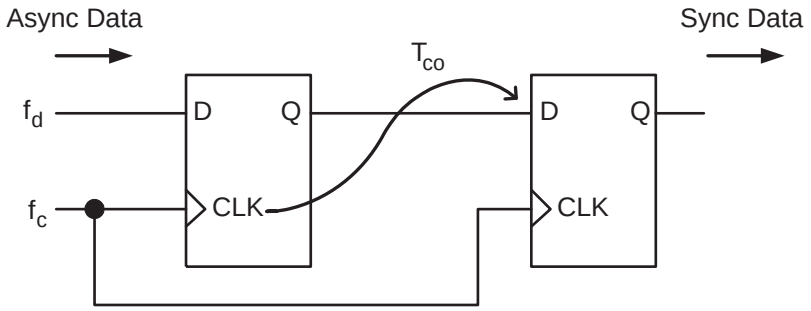

***Figure 1* • Example of Synchronization Circuit**

As mentioned earlier, the aperture represents the likelihood of the flip-flop entering a metastable state. The aperture is defined as a time window within the clock period. Data transitioning inside the aperture will cause the flip-flop output settling time to be greater than $T_{co} + T_{met}$. The aperture is calculated by recording the number of instances in which the settling time exceeds the specified $T_{co} + T_{met}$. The metastability aperture decreases exponentially as the allowed settling time ($T_{co} + T_{met}$) increases:

$$\text{Aperture} = T_o \times e^{-(Tco + Tmet)/\tau}$$

EQ 3

If the data transition occurs within the aperture, the flip-flop will stay metastable beyond the allocated settling time ($T_{co} + T_{met}$); and therefore, the second flip-flop would register invalid data (Figure 1). The probability of an asynchronous data transition is uniformly distributed over the clock period. Therefore, the probability of a single data transition occurring in the metastable aperture is calculated by EQ 4:

$$p = \text{aperture} / T_c$$

EQ 4

where T_c is the clock period.

In each clock cycle, the failure occurs if the data transition time is within the aperture. Therefore, the number of failures in one clock cycle can be derived by EQ 5:

$$n_e = n \times p = n \times (\text{aperture} / T_c)$$

EQ 5

where n_e represents the number of errors per clock cycle, and n is the number of data transitions per clock period (f_d / f_c).

The number of clock cycles in the operation time (N) is the total time divided by the clock period, or

$$N = T_{operation} / T_c$$

EQ 6

Combining EQ 5 and EQ 6 results in the total number of failures per operation time (N_e):

$$N_e = N \times n_e = (T_{operation} / T_c) \times (f_d / f_c) \times (\text{aperture} / T_c)$$

EQ 7

Since $T_c = 1 / f_c$, EQ 7 can be simplified to

$$N_e = T_{operation} \times f_d \times f_c \times \text{aperture}$$

EQ 8

MTBF is defined as the operation time divided by the number of failures, or

$$\text{MTBF} = 1/ (f_d \times f_c \times \text{aperture}) = 1/ (T_0 \times e^{-(Tco + Tmet) / \tau} \times f_d \times f_c)$$

EQ 9

FPGA Metastability Characterization

Like other FPGA manufacturers, to absorb the fixed value the of e^{Tco} term, Microsemi simplifies EQ 9 on page 412 to the following form:

$$MTBF = e^{C2 * Tmet} / (C1 \times f_d \times f_c)$$

EQ 10

where C2 is a constant inversely proportional to the metastability decay constant, and C1 is the proportionality constant, which is similar to aperture.

The FPGA metastability characterization is a series of tests conducted to identify the value of C1 and C2. There are several environmental and test condition factors that influence the characterization. These factors include but are not limited to the rise time of data and clock signals, input voltage levels, and operating voltage and temperature. Moreover, increased system noise due to switching of both internal nodes and I/Os can influence the metastability results. Therefore, it is essential to provide a suitable environment for testing.

Test Design Description

Figure 2 shows a schematic of the test circuit used to characterize the metastability in Microsemi devices. The propagation delay, operating under specified setup and hold time, is measured from the output of flip-flop DFF#1 to the input of flip-flop DFF#3. This value is denoted by EQ 11:

$$T_{min} = T_{cof}(DFF\#1) + T_{delay} + T_{su}(DFF\#3)$$

EQ 11

where T_{delay} is the propagation delay from output of DFF#1 to input of DFF#3, T_{cof} is the clock-to-out delay of DFF#3, and T_{su} represents the setup time requirement of DFF#3. T_{min} corresponds to the T_{co} in EQ 9 on page 412 and is the reference time to which the additional settling time, T_{met}, is added for characterization of metastability.

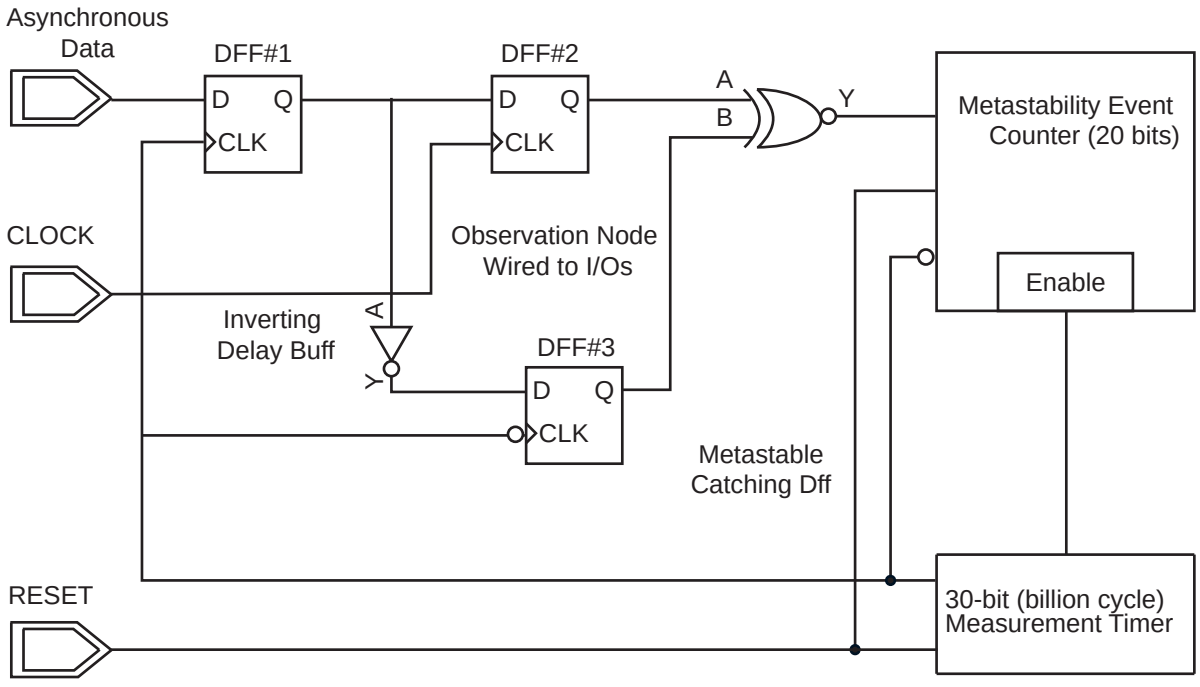

***Figure 2* • Test Circuit**

DFF#2 is clocked on the same edge as DFF#1. Conversely, DFF#3 must resolve the signal driven from the metastable DFF#1 before the falling clock edge. As can be seen in the design in Figure 2, $T_{min} + T_{met}$ is the difference between the rising and falling edge of the clock. Therefore, it can be easily set or

measured by adjusting the duty cycle of the clock signal. A detectable metastable event occurs when DFF#2 and DFF#3 are in the SAME state. In the expected operation, DFF#2 and DFF#3 are in opposite states due to the inverter in the DFF#3 input data path. The XNOR gate allows the event counter to record these metastable events. After a billion clock cycles, the counter is read and the MTBF is calculated.

In this test, T_{min} was resolved to within ±0.01% of the duty cycle at 10 MHz. This translates to an error of ±10 ps.

The other test setup parameters were as follows:

- Clock and data inputs were driven from independent pulse generators (<1 ns rise time).
- Clock input levels were from 0 V to 2.5 V. These levels were required due to the impedance matching of Microsemi's test fixture. Data input levels were 0 V to 3.3 V.
- FPGA power supplies for all tests were at V_{DDP} = 3.3 V and V_{DD} = 2.5 V.

Metastability Measurement Results

EQ 10 on page 413 can be reformed into EQ 12:

$$\ln(MTBF) = C2 \times T_{met} - \ln(C1 \times f_d \times f_c)$$

EQ 12

The plot of EQ 12 is a linear relationship between ln(MTBF) and T_{met}, where C2 is the slope of the line. Figure 3 shows the plot of EQ 12 for ProASIC and ProASIC^{PLUS} FPGA families. C1 and C2 can be calculated from any two data points.

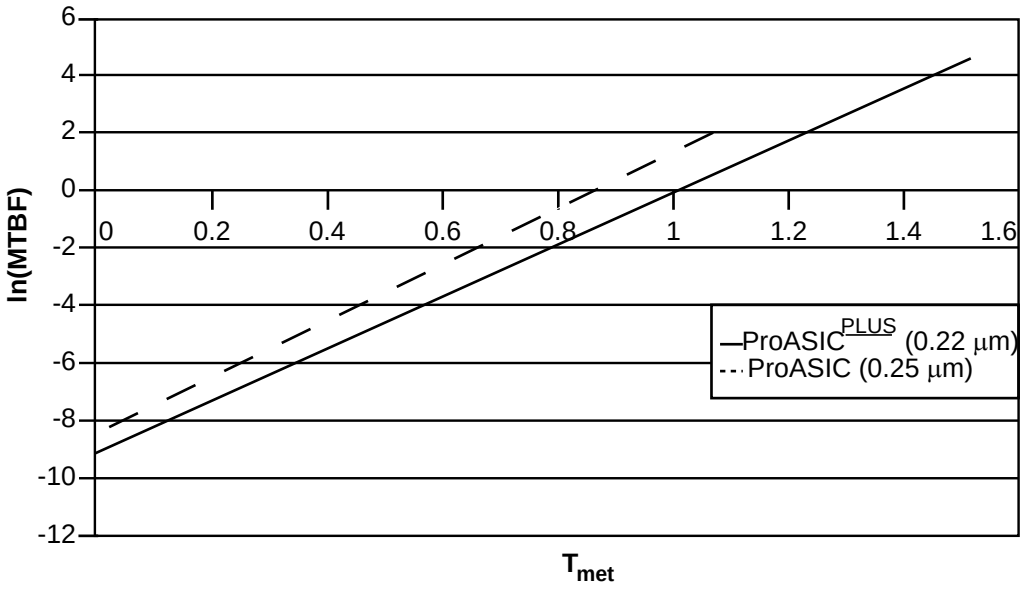

***Figure 3* • Metastability Comparison of Microsemi FPGA Families**

The metastability theory indicates that C1 and C2 are independent of the test clock and data frequency. The test results concur within experimental tolerances. The calculations of C1 and C2 are given in Table 1.

Table 1 • **Metastability Coefficients for Microsemi Flash FPGAs**

f_c = 10 MHz		
Device Family	**C_1 (Hz)**	**C_2 (Hz)**
ProASIC	9.95E–11	1.03E+10
ProASIC^{PLUS}	1.56E–11	9.148E+09
ProASIC3/E Core Registers	9.11E–12	1.57E+10
ProASIC3/E I/O Registers	2.25E–12	1.91E+10

Examples of Metastability Coefficients Usage

Metastability shows a statistical nature, and designers should allow enough additional time (T_{met}) that the likelihood of metastable failure is remote enough to be tolerable by the design specification.

For example, consider that the simple circuit in Figure 1 on page 412 is implemented in a ProASIC^{PLUS} device to synchronize an asynchronous data input to the FPGA. The following parameters are given to designer by either design specification or post-layout timing analysis:

T_{co} = 10 ns, corresponding to a clock frequency of 100 MHz

Asynchronous data transition rate = 12.5 MHz

Tolerable MTBF = 1 year

If the designer does not allow additional sampling time (T_{met} = 0 ns) and run the clock at the rate of 100 MHz, EQ 12 on page 414 will result in MTBF = 51.2 µs. This means that a metastability error will occur at the output of the second flip-flop every 51.2 µs. This value exceeds the required MTBF of one year indicated in the design specification. To meet this requirement, the designer needs to allow additional T_{met} in the sampling time, which can be calculated as follows:

1 year = 365 × 24 × 3,600 = 31,536,000 seconds

ln 31,536,000 = 9.148E+09 × T_{met} – ln (1.56E–11 × 100E6 × 12.5E6) $\geq$ T_{met} = 2.96 ns

Therefore, an additional 3 ns sampling time will fulfill the required MTBF.

List of Changes

The following table lists critical changes that were made in each revision of the chapter.

Date	Changes	Page
June 2011	In Table 1 • Metastability Coefficients for Microsemi Flash FPGAs, the units for C1 and C2 were changed from seconds to Hz (SAR 29148).	415
v1.0 (January 2008)	Table 1 • Metastability Coefficients for Microsemi Flash FPGAs was updated to include ProASIC3/E information.	415
5190062-0	This document was updated to provide a detailed description of the calculations being made.	N/A

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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