

## Introduction [\(Ask a Question\)](#)

This document provides instructions for using the Aurora 8B/10B IP on the PolarFire® Evaluation Board. The PolarFire high-speed transceiver (PF\_XCVR\_ERM) must be configured in PCS 8B10B mode along with the Aurora 8B/10B IP. The AURORA\_TX\_GENERATOR and AURORA\_RX\_CHECKER modules are used to generate and verify data through the AXI4-Stream interface.

The Evaluation Board has two interfaces: SFP+ and SMA. This reference design supports both configurations. The cable must be connected in loopback mode from TX to RX on the board.

## Table of Contents

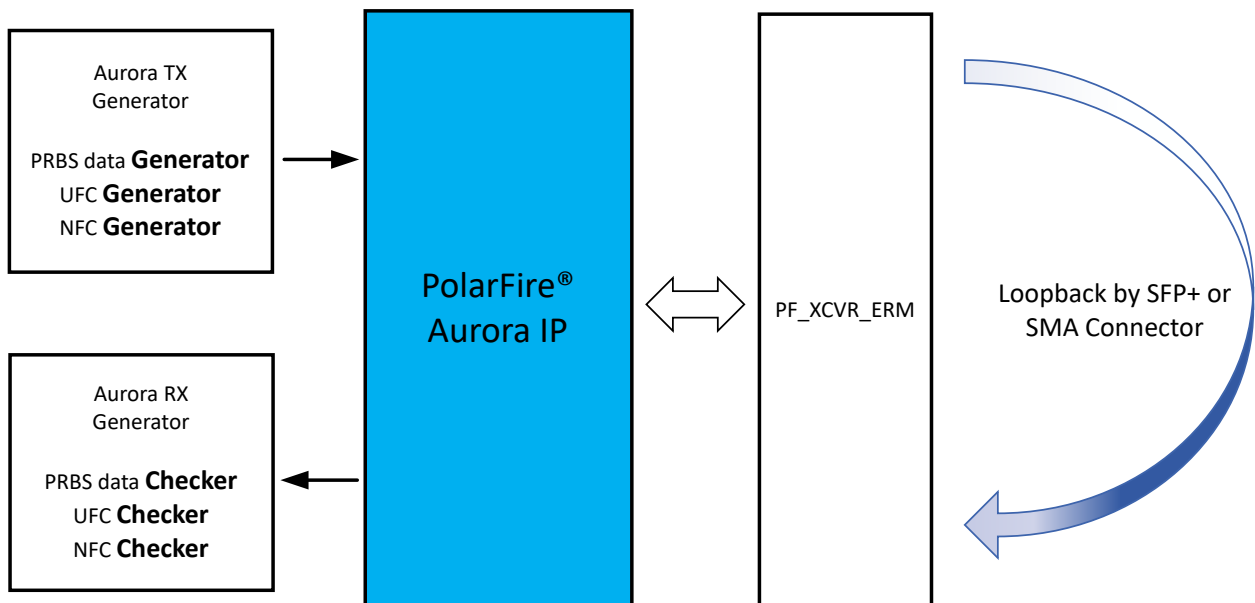
Introduction.....	1
1. Overview.....	3
2. Reference Design Specifications.....	4
3. Design Information.....	5
3.1. Aurora Tx Generator.....	5
3.2. Aurora Rx Checker.....	6
3.3. Transceiver Configuration.....	6
4. Libero Project.....	8
4.1. Timing Constraints.....	8
4.2. Interface Constraints.....	8
5. Simulation.....	10
6. Debug and Testing.....	12
7. Revision History.....	16
Microchip FPGA Support.....	17
Microchip Information.....	17
Trademarks.....	17
Legal Notice.....	17
Microchip Devices Code Protection Feature.....	18

## 1. Overview (Ask a Question)

The Aurora 8B/10B IP uses AXI4-Stream as the user interface for communication. This reference design includes two modules, AURORA\_TX\_GENERATOR and AURORA\_RX\_CHECKER, for testing. The high-speed transceiver block supports data rates ranging from 250 Mbps to 12.7 Gbps. The transceiver (PF\_XCVR\_ERM) module integrates multiple functional blocks to enable high-speed serial data transfer within the FPGA. The transceiver used in the Aurora 8B/10B applications has a bandwidth limited to a line rate range of 0.5 Gb/s to 6.6 Gb/s.

The Aurora 8B/10B IP supports a 32-bit data width and single transceiver lanes. This reference design can be implemented on two Microchip PolarFire boards to enable full-duplex data transfer.

**Figure 1-1.** Aurora 8B/10B IP Reference Design Block Diagram



## 2. Reference Design Specifications [\(Ask a Question\)](#)

This section provides a list of reference design specifications.

- Full-duplex mode
- Single-lane channel
- Data rate: 3.125 Gbps
- Payload Data Unit (PDU): 32-bit data width
- Test User Flow Control (UFC) and Native Flow Control (NFC)

### 3. Design Information [\(Ask a Question\)](#)

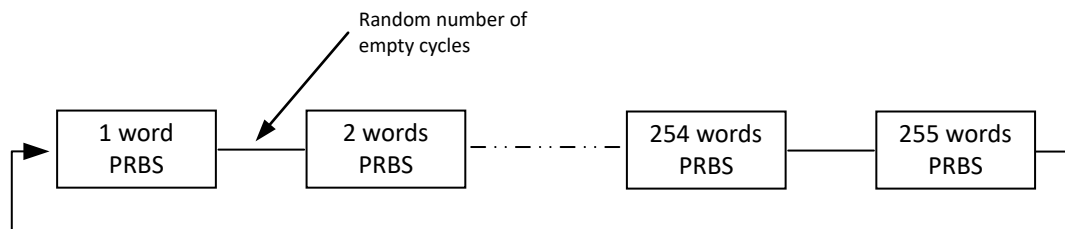
This section provides an overview of the modules included in the design.

#### 3.1. Aurora Tx Generator [\(Ask a Question\)](#)

When the LANE and CHANNEL are successfully initialized, the `AURORA_TX_GENERATOR.CHANNEL_UP` signal is asserted. The generator then starts producing test patterns and sends them to the Aurora 8B/10B IP through the AXI4-Stream interface.

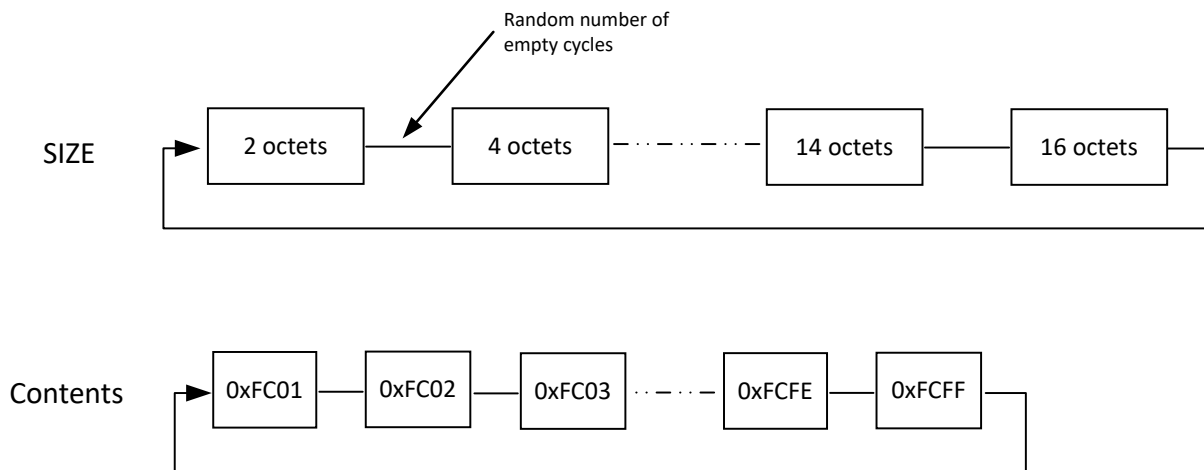
- **Data Transmission:** The PRBS data pattern is used to test the TX user interface. The data word size increases incrementally in each frame, ranging from 1 to 255 (1 word = 32 bits). A short random number of cycles is inserted between frames.

Figure 3-1. Data Test Sequence



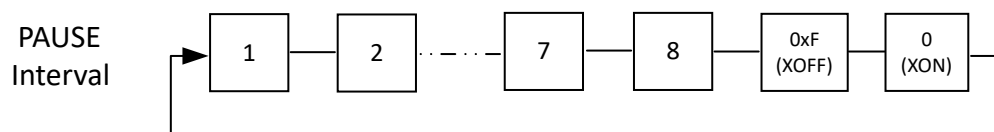
- **UFC Message Transmission:** Pre-set values are used to test the TX UFC user interface. According to the Aurora 8B/10B specification, the UFC size range is an even number of octets, between 2 and 16.

Figure 3-2. UFC Test Sequence



- **NFC Message Transmission:** The sequence of pause numbers follows the pattern 1 to 8, then 0xF and finally 0. According to the Aurora 8B/10B specification, the NFC data range is from 1 to 8. A value of 0xF instructs the channel partner to stop transmitting data, while a value of 0 instructs it to resume transmission.

Figure 3-3. NFC Test Sequence



### 3.2. Aurora Rx Checker [\(Ask a Question\)](#)

After the LANE and CHANNEL are successfully initialized, the CHECKER module starts verifying the data received from the Aurora 8B/10B IP through the AXI4-Stream interface.

The following table provides port information. These ports indicate respective data mismatch errors.

**Table 3-1.** Aurora Rx Checker

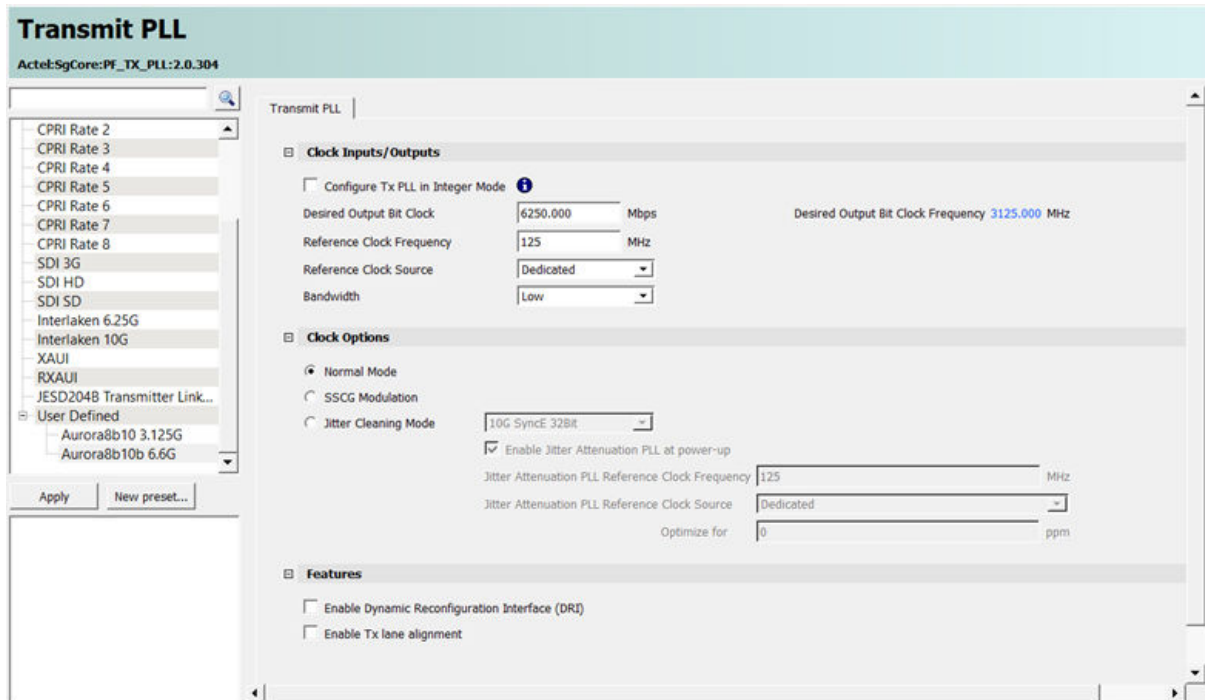
Signal Hierarchy	Description
AURORA_RX_CHECKER.ERR_PDU	Indicates a mismatch in the received PDU data.
AURORA_RX_CHECKER.ERR_UFC	Indicates a mismatch in the received UFC message.
AURORA_RX_CHECKER.ERR_NFC	Indicates a mismatch in the received NFC message.

### 3.3. Transceiver Configuration [\(Ask a Question\)](#)

PolarFire Aurora 8B/10B IP does not include transceiver PMA and PCS. The following figure shows the configuration of Transceiver IP in Libero® design.

1. The PolarFire Evaluation Board provides a 125 MHz clock source. Configure the PF\_TX\_PLL IP to generate a 6250 Mbps bit clock for PF\_XCVR\_ERM.

**Figure 3-4.** Transmit PLL



2. Configure PF\_XCVR\_ERM for full-duplex operation with a single lane and a data rate of 3.125 GHz.
3. Configure the PCS interface width to 32 bits with 8B/10B encoding and decoding.

Figure 3-5. Transceiver Interface

### Transceiver Interface

Microsemi: SystemBuilder: PF\_XCVR\_ERM

- SGMII
- QSGMII
- CPRI Rate 1
- CPRI Rate 2
- CPRI Rate 3
- CPRI Rate 4
- CPRI Rate 5
- CPRI Rate 6
- CPRI Rate 7
- CPRI Rate 8
- SDI 3G
- SDI HD
- SDI SD
- Interlaken 6.25G
- Interlaken 10G
- XAUI
- RXAUI
- JESD204B Receiver Link with ...
- JESD204B Transmitter Link wi...
- User Defined
  - Aurora8b10 6.6G
  - Aurora8b10b

Apply    New preset...

**General**

Transceiver mode: Tx and Rx (Full Duplex)     Enhanced receiver management

Number of lanes: 1    Receiver calibration: None (CDR)  Incrementally recalibrate data eye  Incrementally recalibrate DFE coefficients

**PMA Settings**

TX data rate: 3125 Mbps	RX data rate: 3125 Mbps
TX clock division factor: 2	RX CDR lock mode: Track to data
TX PLL base data rate: 6250.000 Mbps	RX CDR reference clock source: Dedicated
TX PLL bit clock frequency: 3125.000 MHz	RX CDR reference clock frequency: 125.0 MHz
	RX JA clock frequency: 78.125 MHz

**PCS Settings**

TX PCS-Fabric interface width: 32 bits	RX PCS-Fabric interface width: 32 bits
TX FPGA interface frequency: 78.125 MHz	RX FPGA interface frequency: 78.125 MHz

**PMA Mode**

Enable CDR Bit-slip port

8b10b Encoding/Decoding

64b6xb Gear Box

<input checked="" type="checkbox"/> 64b66b	<input type="checkbox"/> 64b67b
<input type="checkbox"/> Enable Disparity	<input checked="" type="checkbox"/> Enable BER monitor state machine
<input checked="" type="checkbox"/> Enable Scrambler/Descrambler	<input type="checkbox"/> Enable 32 bits data width

**Soft PIPE Interface**

Protocol: PCIe Gen1 (2.5 Gbps)

**Clocks and Resets**

Interface Clocks

Use as PLL reference clock

TX clock: Regional    RX clock: Regional

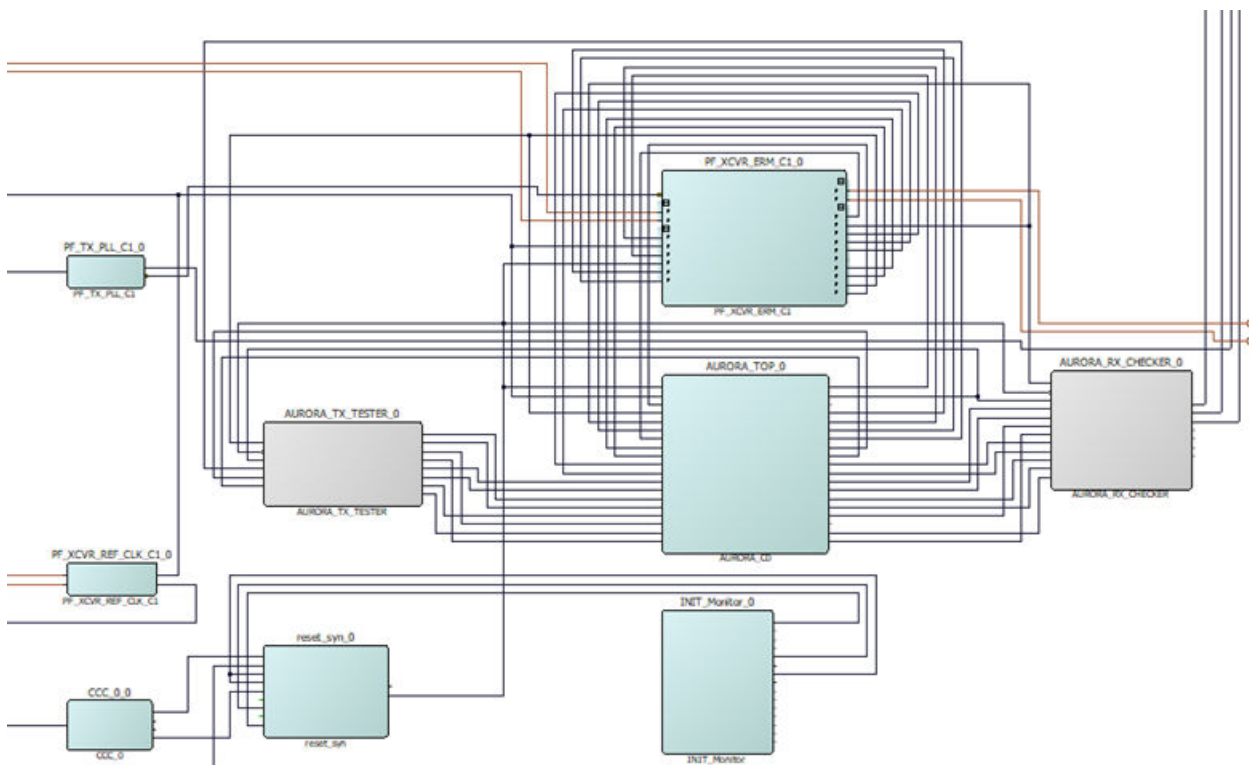
Interface Resets

## 4. Libero Project [\(Ask a Question\)](#)

In addition to the main functional block, there are additional modules such as CCC, `reset_syn` and `INIT_Monitor`, which are responsible for generating the system clock and reset.

The following figure shows the top-level Libero design of the high-speed data transfer using Aurora 8B/10B IP.

**Figure 4-1.** Libero Project



### 4.1. Timing Constraints [\(Ask a Question\)](#)

The following constraint describes the frequency of `SYS_CLK` is 125 MHz, `TX_CLK` and `RX_CLK` are 78.125 MHz.

The false path `ARSTN` is an asynchronous signal.

```
create_clock -name {REF_CLK_PAD_P} -period 8 -waveform {0 4} [ get_ports { SYS_CLK } ]
create_clock -name {PF_XCVR_ERM_C1_0/I_XCVR/LANE0/TX_CLK_R} -period 12.8 [ get_ports
{ TX_CLK } ]
create_clock -name {PF_XCVR_ERM_C1_0/I_XCVR/LANE0/RX_CLK_R} -period 12.8 [ get_ports
{ RX_CLK } ]

set_false_path -from [ get_ports { ARSTN } ]
set_clock_groups -asynchronous -group [ get_clocks { PF_XCVR_ERM_C1_0/I_XCVR/LANE0/
TX_CLK_R } ]
set_clock_groups -asynchronous -group [ get_clocks { PF_XCVR_ERM_C1_0/I_XCVR/LANE0/RX_CLK_R } ]
```

### 4.2. Interface Constraints [\(Ask a Question\)](#)

This section describes interface constraints.

- Constraints for SFP+ connector

```
set_io -port_name LANE0_RXD_N -pin_name AD30 -DIRECTION INPUT
set_io -port_name LANE0_RXD_P -pin_name AD29 -DIRECTION INPUT
```

```
set_io -port_name LANE0_TXD_N -pin_name AE32 -DIRECTION OUTPUT  
set_io -port_name LANE0_TXD_P -pin_name AE31 -DIRECTION OUTPUT
```

- Constraints for SMA connector

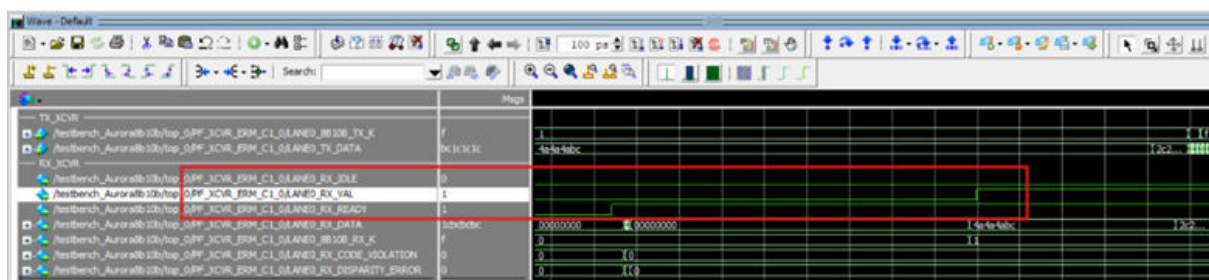
```
set_io -port_name LANE0_RXD_N -pin_name AC32 -DIRECTION INPUT  
set_io -port_name LANE0_RXD_P -pin_name AC31 -DIRECTION INPUT  
set_io -port_name LANE0_TXD_N -pin_name AD34 -DIRECTION OUTPUT  
set_io -port_name LANE0_TXD_P -pin_name AD33 -DIRECTION OUTPUT
```

## 5. Simulation [\(Ask a Question\)](#)

A loopback simulation testbench is provided. The following key observations can be made from the waveform:

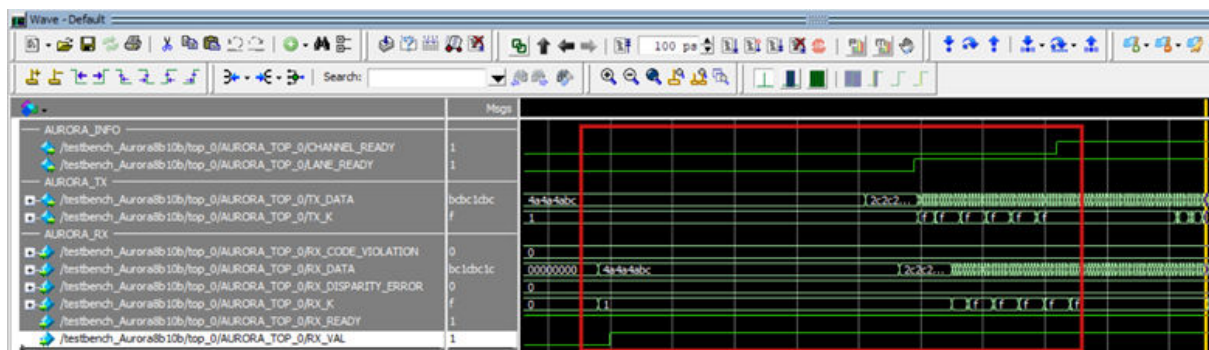
- When both `PF_XCVR_ERM_RX_VAL` and `PF_XCVR_ERM_RX_READY` are asserted, it indicates that the receiver of `PF_XCVR_ERM` has completed initialization. The Aurora 8B/10B IP will start operating upon receiving these signals.

Figure 5-1. Simulation



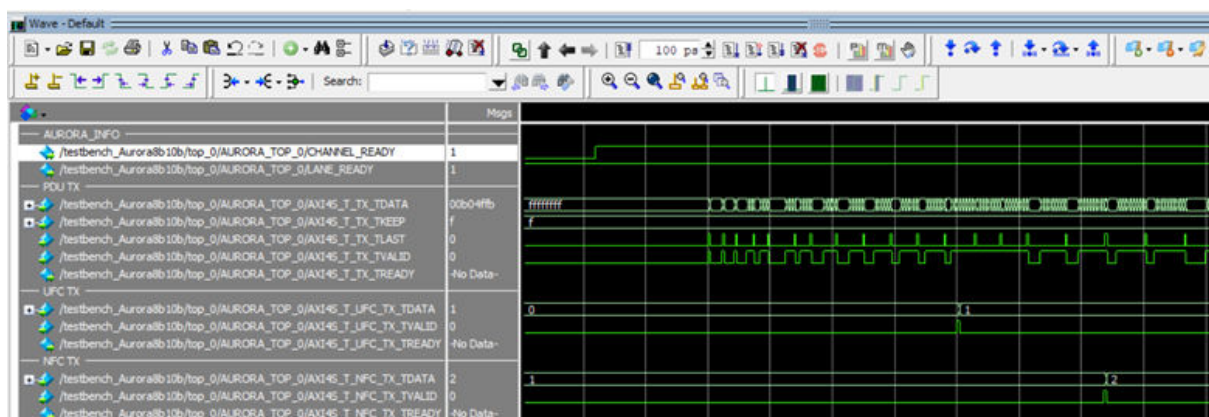
- During the time interval from `RX_VAL` to `CHANNEL_READY`, the Aurora 8B/10B IP undergoes initialization and verification. The user application system must wait until `CHANNEL_READY` is asserted before starting operation.

Figure 5-2. CHANNEL\_READY is Asserted before Starting Operation



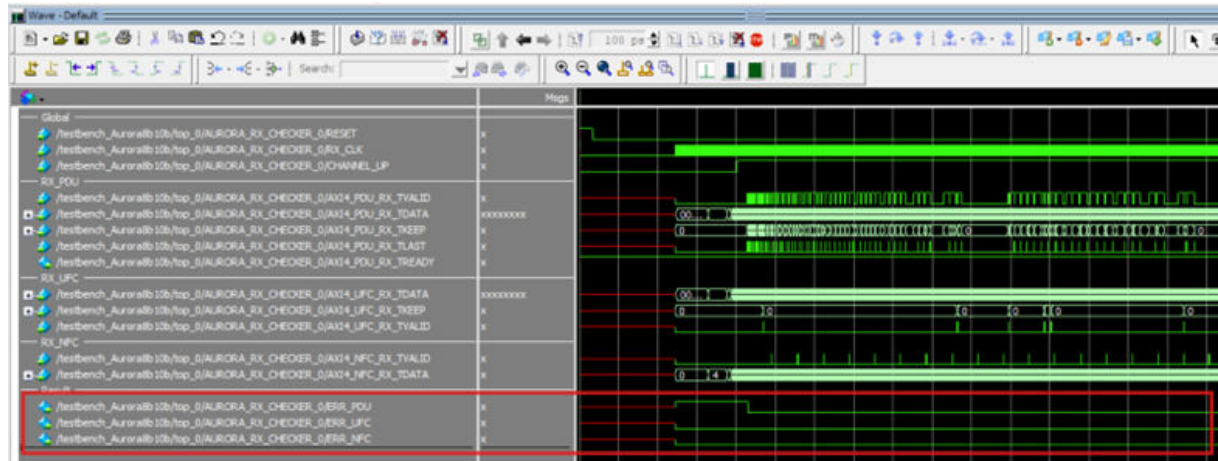
- The `TX_GENERATOR` module starts transmitting test patterns to Aurora 8B/10B IP after `CHANNEL_READY` is asserted.

Figure 5-3. CHANNEL\_READY is Asserted



- The AURORA\_RX\_CHECKER module starts verifying the received data after CHANNEL\_UP is asserted.
- The PDU, UFC and NFC data are continuously checked. The ERR\_PDU, ERR\_UFC and ERR\_NFC signals must remain low; otherwise, a data mismatch is detected.

Figure 5-4. Data Mismatch Detected



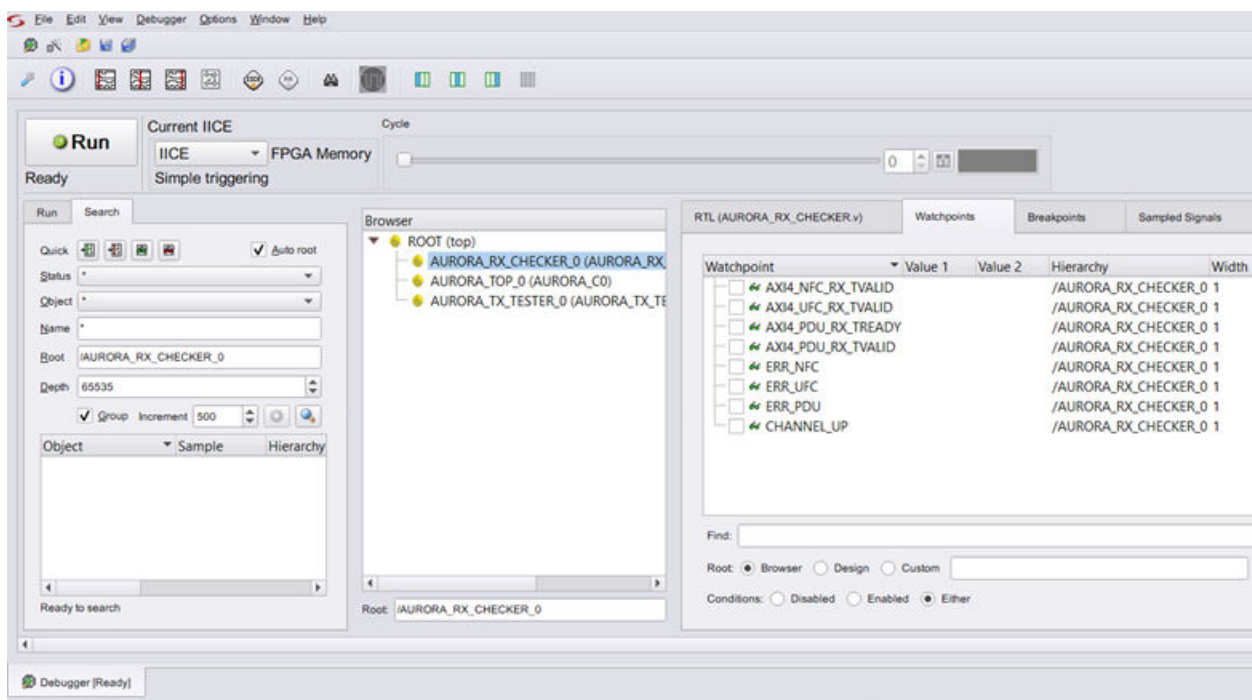
## 6. Debug and Testing (Ask a Question)

Use the Identify® Debug Design tool to monitor signals in the design.

1. CHANNEL\_UP
  - This signal should be asserted after the cable is plugged in and the initialization process is complete.
2. ERR\_PDU / ERR\_UFC / ERR\_NFC
  - These signals should always remain low.
  - Set a trigger in tool to monitor for errors.
3. Status LEDs
  - LED4: DATA error. LED illumination indicates an error for data.
  - LED5: UFC error. LED illumination indicates an error for UFC.
  - LED6: NFC error. LED illumination indicates an error for UFC.
  - LED7: CHANNEL READY. LED illumination indicates successful initialization.

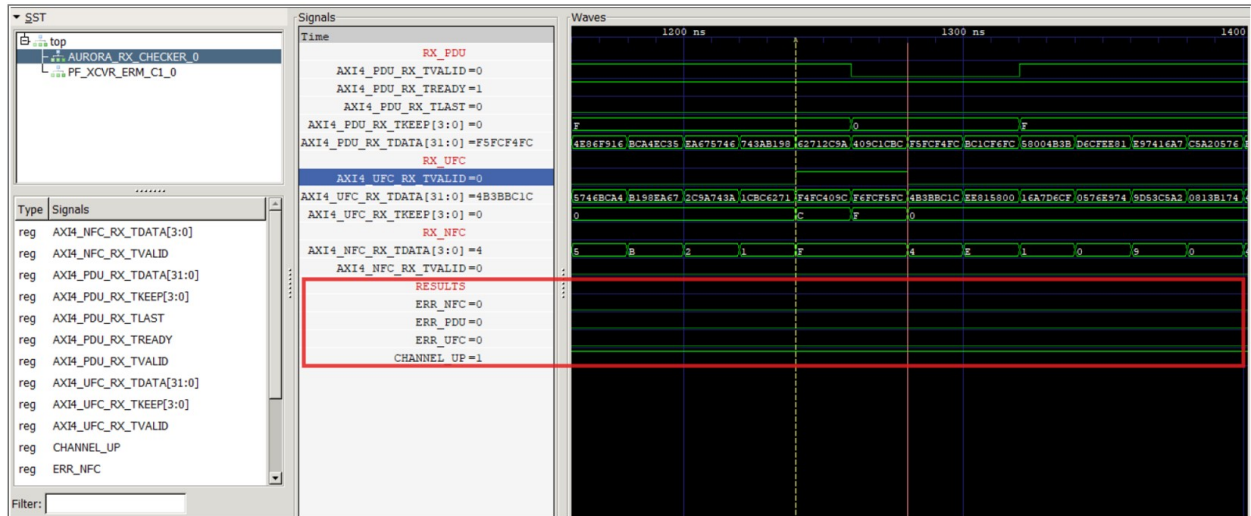
The following figure shows the Identify Debug Design Tool.

**Figure 6-1.** Debug and Testing



The following figure shows results in the waveform viewer.

Figure 6-2. Monitor Error



To test the hardware setup, follow the instructions below:

1. Close jumper J46.
2. Connect SPF+ and optical cable in loop-back mode.
3. Observe the status of LEDs.

The following figure shows the setup of a PolarFire development board.

Figure 6-3. Board Setup

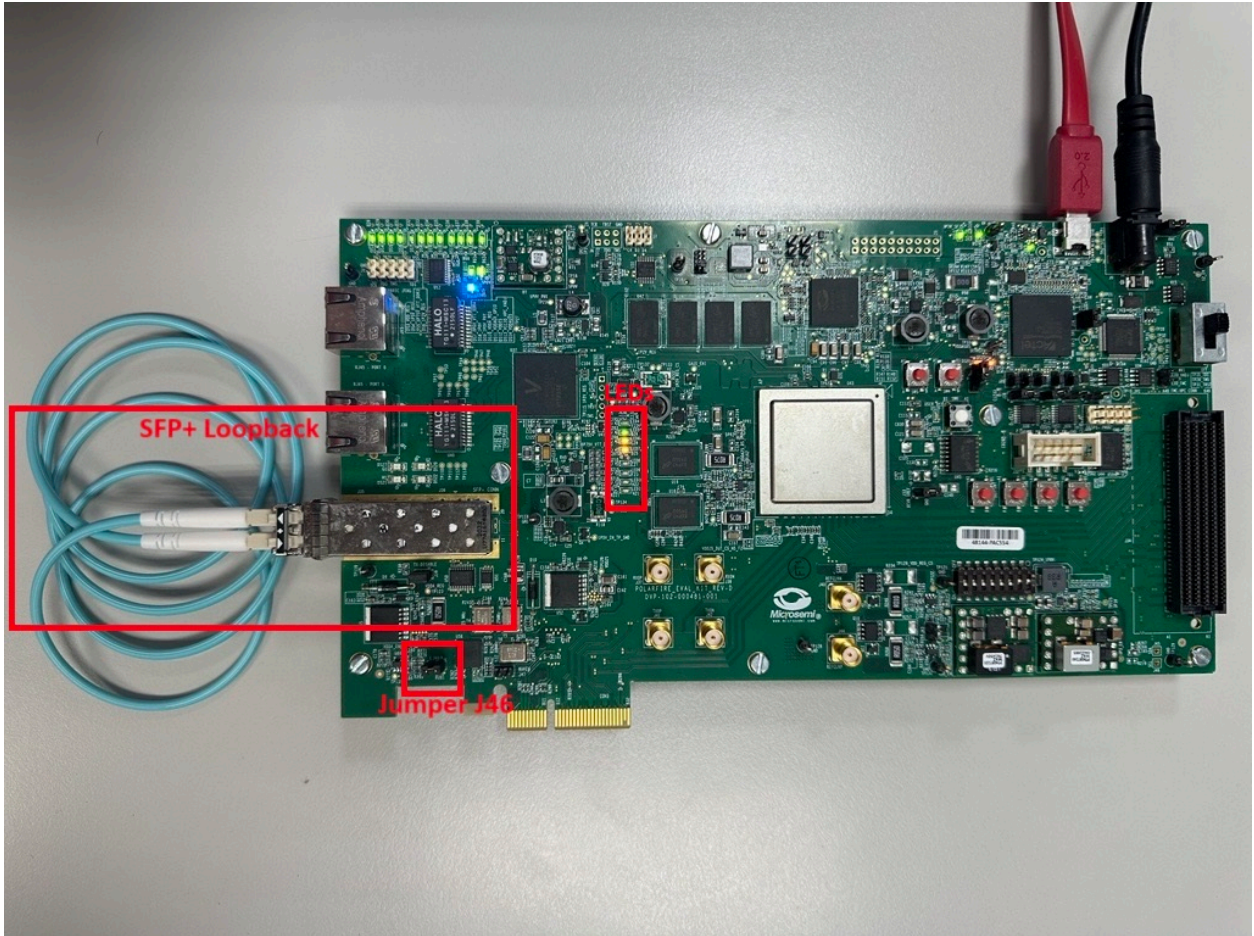
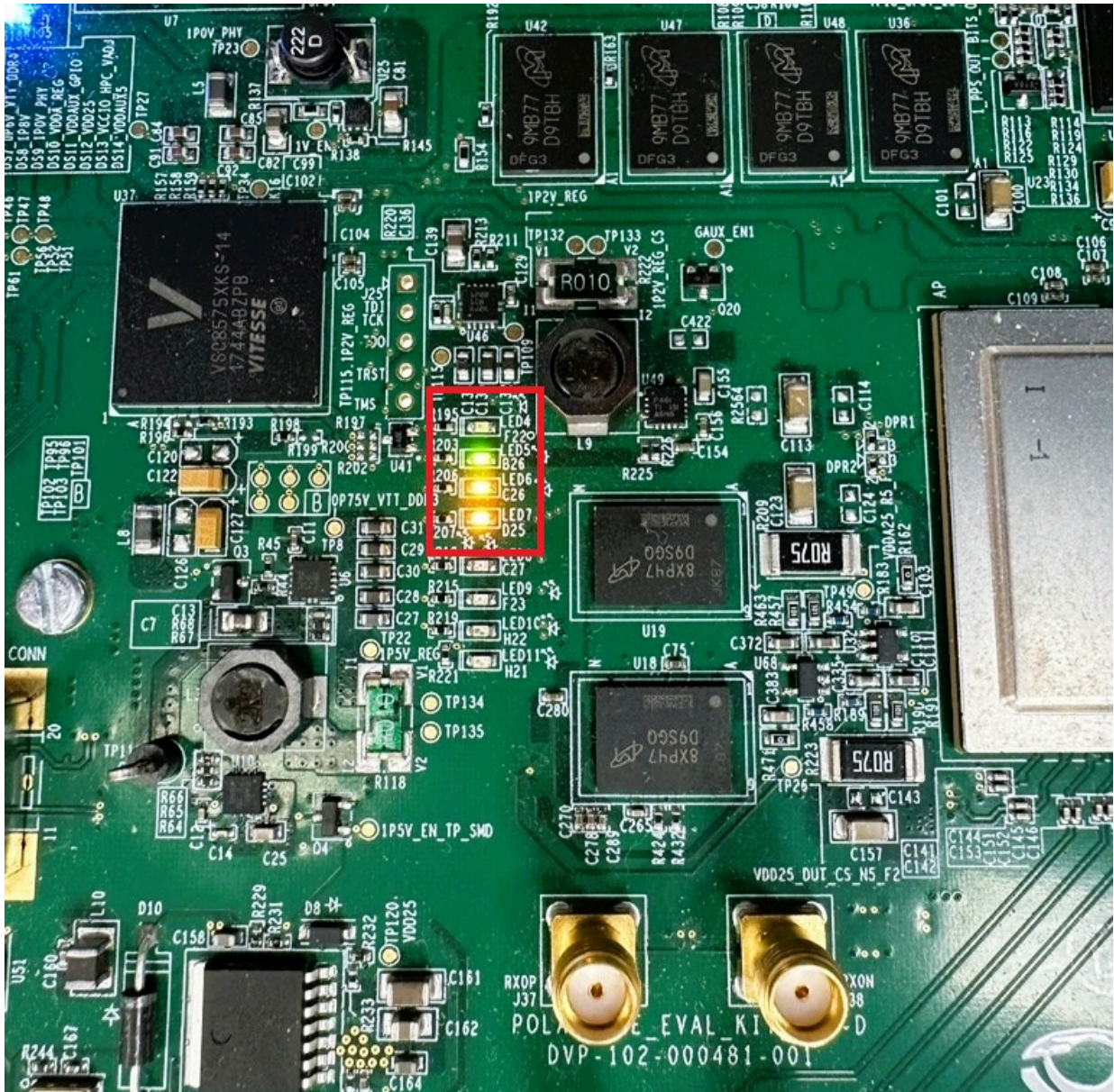


Figure 6-4. Status of LEDs



**➔ Important:**

- LED4: PDU error status, ON indicates, an error has detected.
- LED5: UFC error status, ON indicates, an error has detected.
- LED6: NFC error status, ON indicates, an error has detected.
- LED7: Channel ready status, ON indicates, the channel has initialized.

## 7. **Revision History** [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	05/2025	Initial revision.

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