AN4364

PolarFire® FPGA SFP+ Module

Introduction

Microchip's 10G optical SFP+ module is a system-level optical transceiver solution built with the lowest power, smallest form factor, and highly secure PolarFire FPGA.

This application note describes how the PolarFire FPGA can be used in building an SFP+ module and provides guidelines to:

- Build an FPGA based SFP+ module within the given small form factor.
- Design an efficient power integrity for the module and to design a high-performance signal integrity for the high-speed traces.

PolarFire FPGA SFP+ Features

PolarFire FPGAs provide the following features required for the data communication applications.

- Small form factor with a 11 mm x 14.5 mm
- Mid-range device variant (MPF200 FPGA) containing 192K LEs (DFFs + LUTs)
- Low-power advantages required for SFP/SFP+ based applications
- Highly secure and reliable with in-line encryption
- High-performance transceivers at 12.7G
  Thus, PolarFire FPGA-based smart SFP/SFP+ applications saves design time and cost without compromising performance. SFP+ applications around Routers, OAM, OLT/ONU, OTN, 1588, SyncE, and SDN can be built using PolarFire FPGAs.

  For more information about the PolarFire FPGA family, see PolarFire FPGAs.

  The MPF200T-FCSG325 device is used in the SFP+ module. MPF200 includes 192K LEs (DFFs + LUTs) and comes with a 11 mm × 14.5 mm form factor, which makes this device package the best fit for SFP+ applications.

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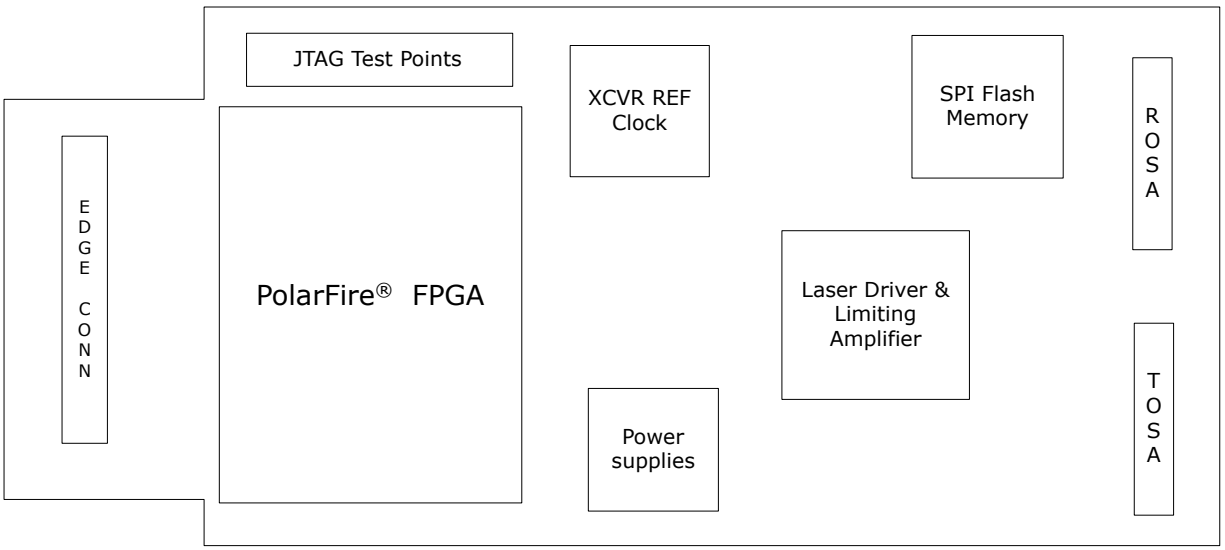
1. Block Diagram

The following block diagram shows the components of the SFP+ module.

Figure 1-1. Block Diagram



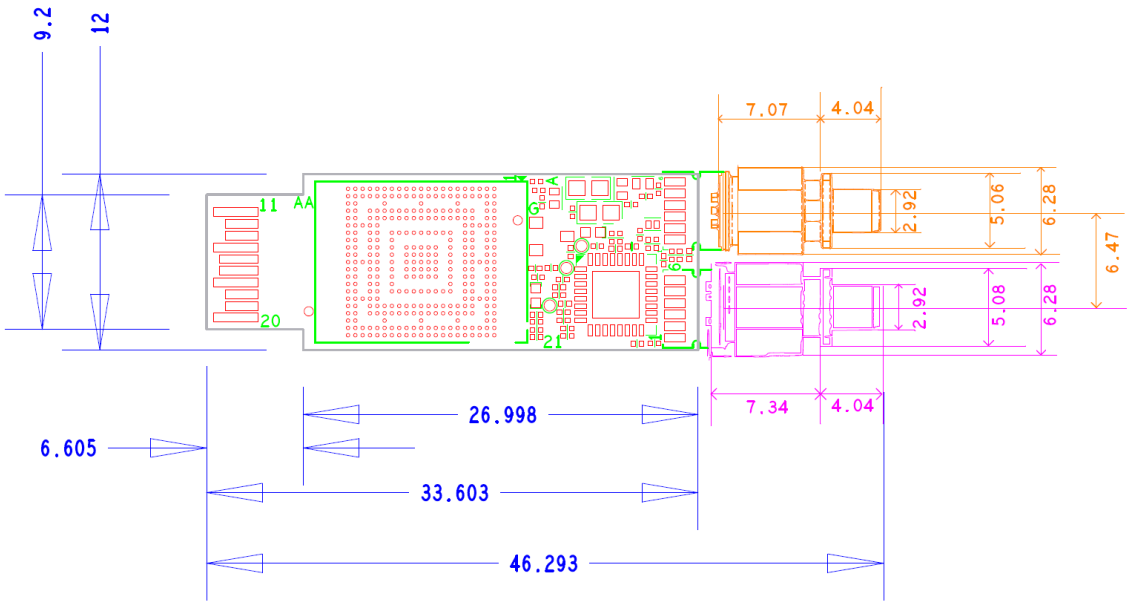
The SFP+ module contains the following components and provisions:

- PolarFire MPF200T-FCSG325 FPGA
- PolarFire FPGA auxiliary circuit for power-up
- Clocking and programing circuit
- Line drivers
- Limiting amplifiers
- Optical communication:
  - Receiver optical sub-assembly (ROSA) required for optical communication
  - Transmitter optical sub-assembly (TOSA) required for optical communication
- Provision for one high-speed serial TX/RX going form PolarFire FPGA to line driver/amplifier
- A few side-band signals to control other circuit
- Edge connector

2. SFP+ Module Dimensions

The module outline dimensions are shown in the following figure.

Figure 2-1. Module Outline Dimensions

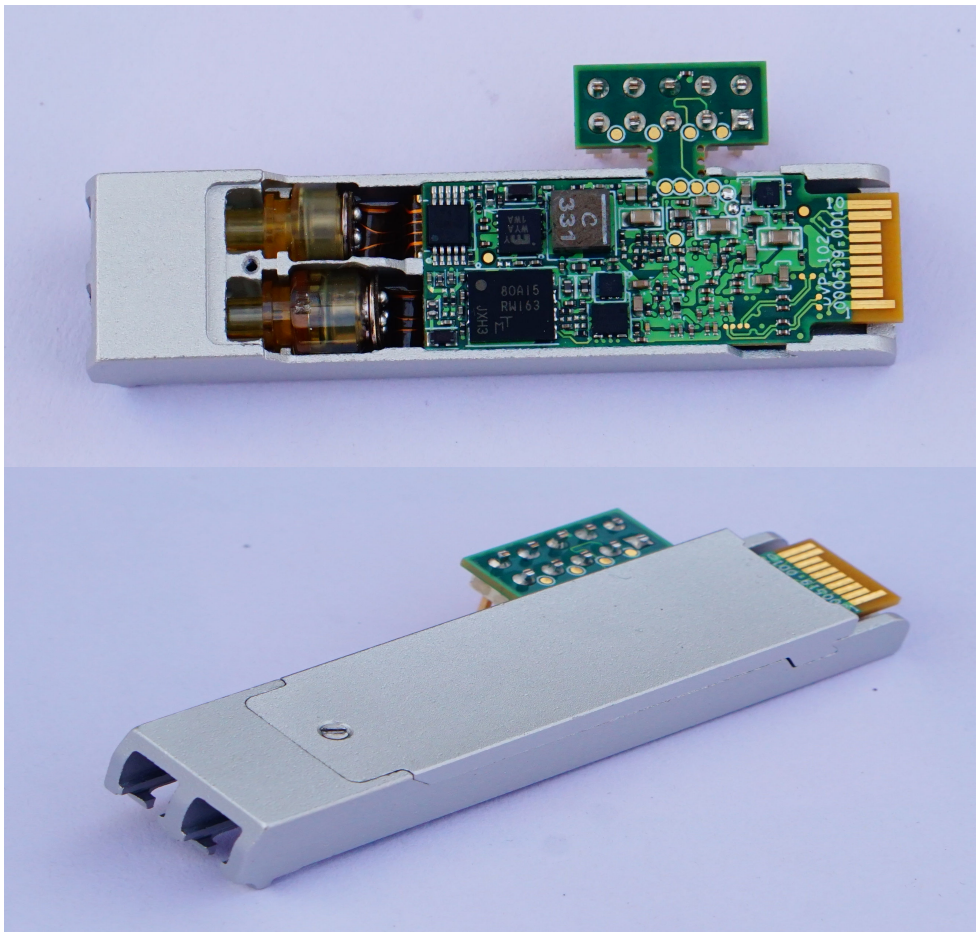


Note: All the dimensions in the figure are in mm.

For more information about the SFP+ from factor, see the SFF-8432 specification.

The following figure shows the SFP+ module with casing.

Figure 2-2. SFP+ Module with Casing



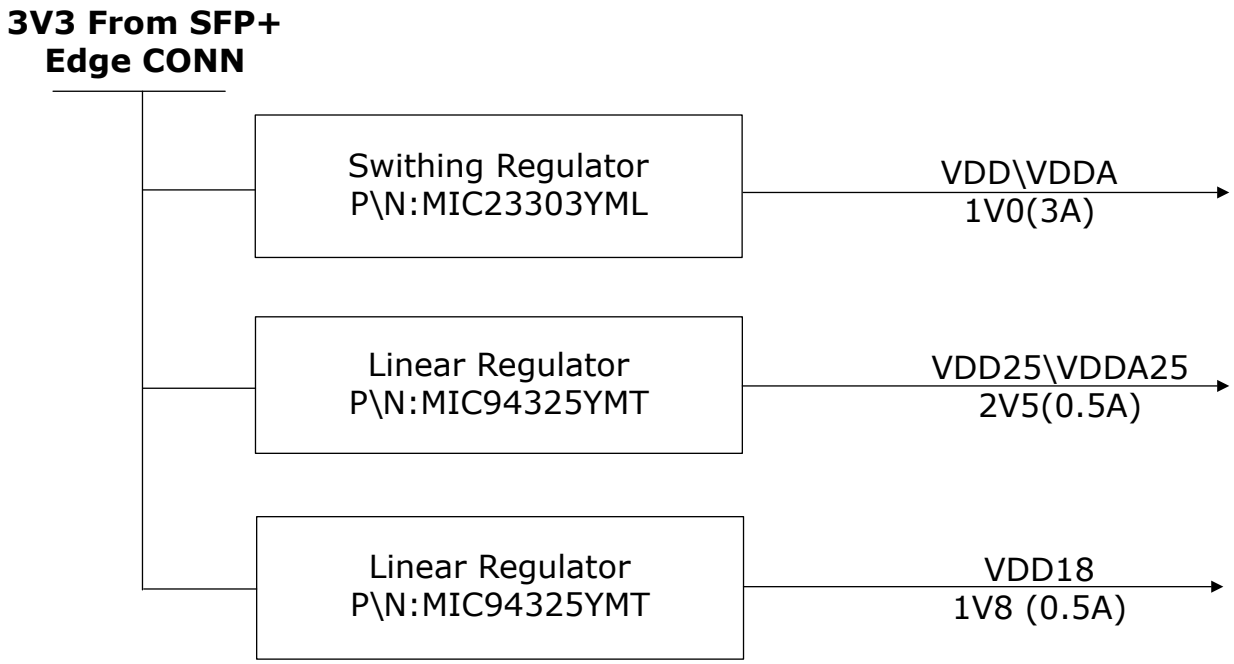
3. Hardware Details

This chapter describes the different components used to build a PolarFire FPGA based SFP+ Module.

3.1 Power Regulation and Consumption

The PolarFire FPGA requires core current (VDD) and transceiver current (VDDA) at 1V0. Other Voltage rails VDD25 and VDDA25 at 2V5, and VDD18 at 1V8 are shown in the following figure. The VDD depends on the size of the design programmed on the FPGA.

Figure 3-1. Power Regulation



For a typical SFP+ application, the core current lies between 1A to 2A. It is highly recommended to check the power consumption using Microchip Power Estimator for different rails before finalizing the power numbers because it may vary with the design.

The following table lists the recommended decoupling capacitors to be used for the PolarFire device.

Table 3-1. Recommended De-coupling Capacitors

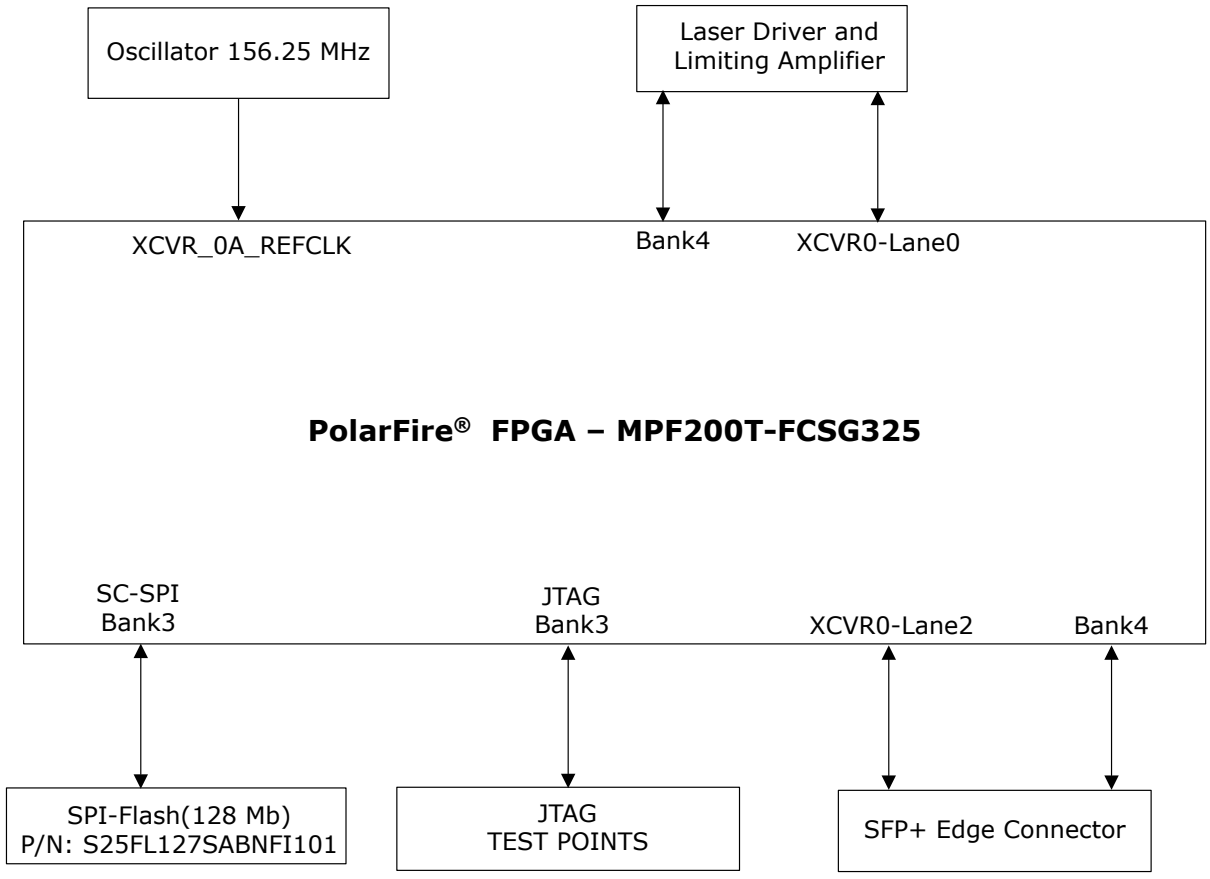
Pin Name	Ceramic Capacitors					
	4.7 µF	0.01 µF	0.1 µF	4.7 µF	10 µF	47 µF
VDD	—	2	2	—	—	2
VDDA	3	1	5	—	1	—
VDD18	—	—	2	—	1	1
VDD25	—	—	5	—	1	—
VDDA25	—	—	4	—	1	—
VDDI3	—	—	2	—	—	—
VDDI4	—	—	2	—	1	—

.....continued						
Pin Name	Ceramic Capacitors					
	4.7 µF	0.01 µF	0.1 µF	4.7 µF	10 µF	47 µF
VDD_XCVR_CLK	—	—	2	—	—	—
VDDAUX4	—	—	2	1	—	—

3.2 FPGA Block Diagram

The following hardware block diagram shows the typical architecture of an FPGA based SFP+ module.

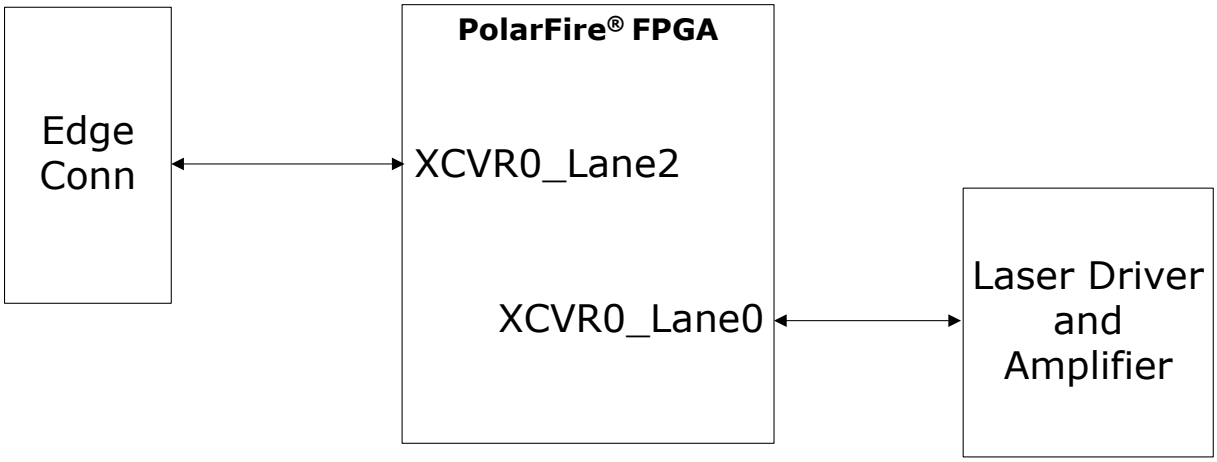
Figure 3-2. FPGA Block Diagram



3.3 Transceiver Design

The following figure shows how the transceiver connects to the edge connector, Laser driver, and the amplifier circuit.

Figure 3-3. Transceiver Connections



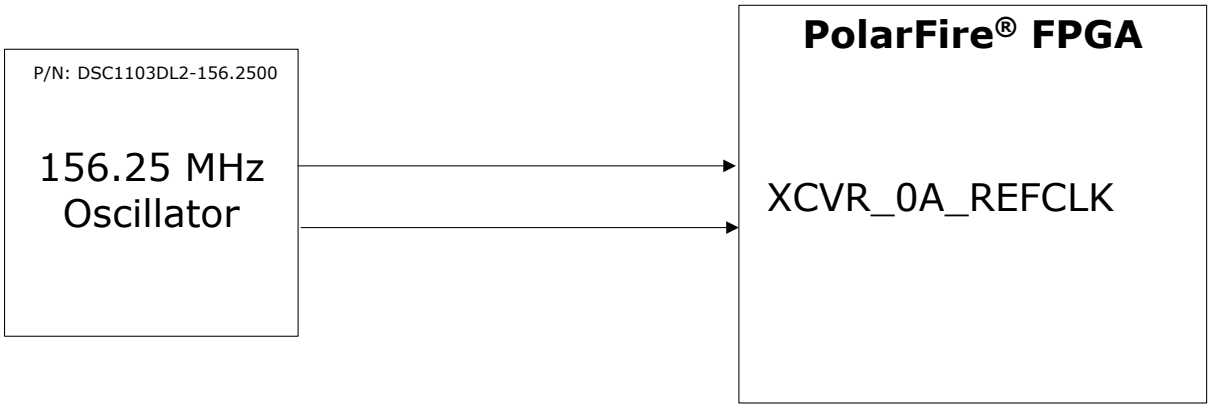
As shown in the preceding figure, the edge connector interfaces with Lane 2 of the PolarFire XCVR block, and the Laser Driver and amplifier unit interfaces with Lane 0.

For more information about the PolarFire Transceiver, see PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide.

3.4 Transceiver Reference Clock Design

A 156.25 MHz oscillator is available on the module to provide reference clock to the PolarFire transceiver block at the XCVR_0A_REFCLK pin. The oscillator output is standard LVDS. For more information about the electrical characteristics and supporting standards of the reference clock, see DS0141: PolarFire FPGA Datasheet.

Figure 3-4. XCVR REFCLK to FPGA



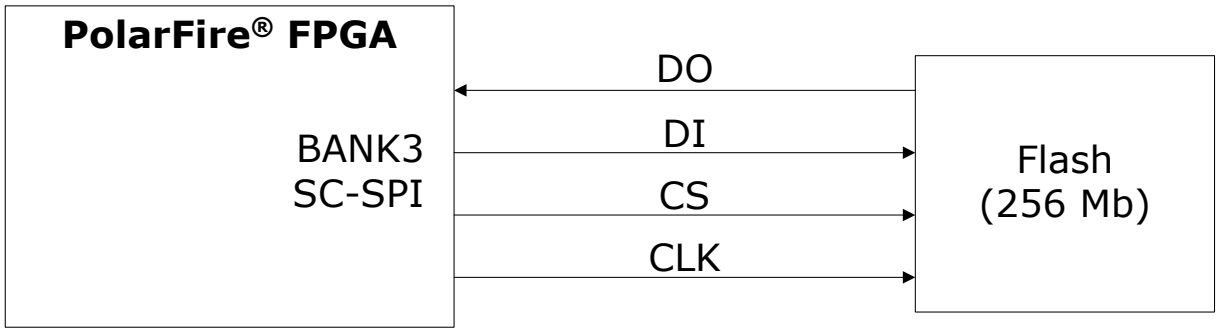
3.5 FPGA Programming Interface Design

PolarFire FPGA can be programmed through SPI. Test points are available for JTAG signals only for debug purpose. The following section describes the SPI programming interface.

3.5.1 SPI Programming

In the SPI programming scheme, the PolarFire FPGA on the SFP+ module programs itself from the SPI Flash. SPI supports in-application programming (IAP) and auto-update. The following figure shows the SPI programming scheme.

Figure 3-5. SPI Programming Scheme



To enable IAP programming, the following FPGA pins must be set high.

- A10 (SC_SPI_ENABLE)
- A9 (SC_IO_CFG_INTERFACE)

The SPI Flash specifications on the module are as follows:

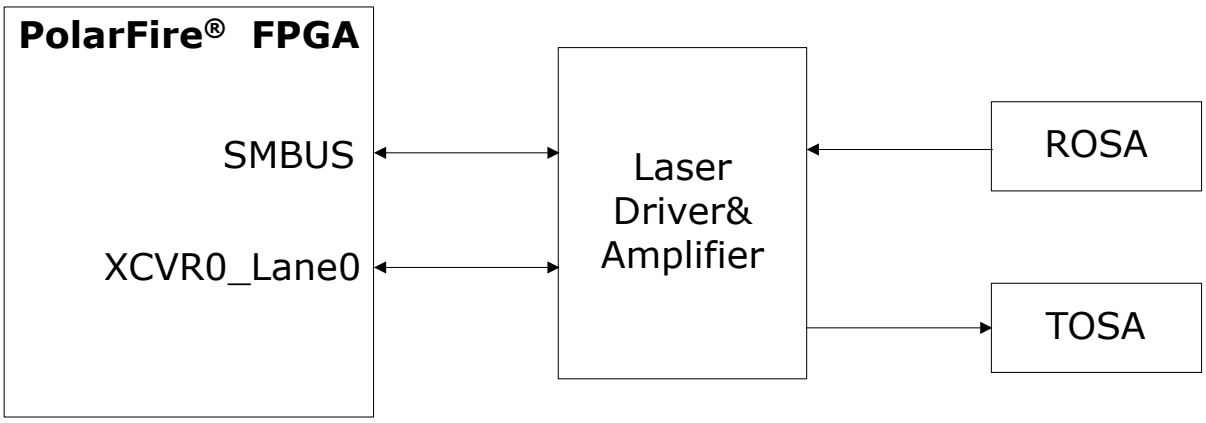
- NOR Memory IC
- Density: 256 Mb (32M x 8)
- Voltage: 2.7 V to 3.6 V (MT25QL256ABA1EW7-0SIT)
- SPI mode support: Modes 0 and 3
- Dedicated BANK: 3

For more information on FPGA programming, see PolarFire FPGA and PolarFire SoC FPGA Programming User Guide.

3.6 Laser Driver and Limiting Amplifier

The module contains a combination of VCSEL driver and limiting amplifier with a 3-wire digital control interfaced from FPGA. This 3-wire interface enables the FPGA to access the registers of the Laser driver and amplifier.

Figure 3-6. Optical Interface



3.7 List of Major Components

The following table lists the major components required for building the total system solution.

Table 3-2. List of Major Components

Sr. No.	Part Number	Description
1	MPF200T-FCSG325	PolarFire FPGA - 200K Logic elements (4 LUT + DFF)
2	MAX3798ETJ+	Limiting Amplifier and VCSEL Driver, TQFN-EP-32
3	DSC1103DL2-156.2500	MEMS OSC XO 156.25 MHz LVDS SMD
4	RP85-LCT2HA-FI-OS	10 Gbps GaAs PIN PD LC-ROSA with Preamp
5	TP85-LCP1HA-FA-OS	850 nm 10 Gbps VCSEL LC-TOSA
6	MT25QL256ABA1EW7-0SIT TR	IC FLASH 256MBIT SPI 8WPDFN
7	MIC23303YML-T5	IC REG BUCK ADJUSTABLE 3A 12DFN
8	MIC94325YMT-TR	IC REG LIN POS ADJ 500MA 6TDFN

4. Hardware Design Details

This chapter shows the placement of the system solution components on the PCB.

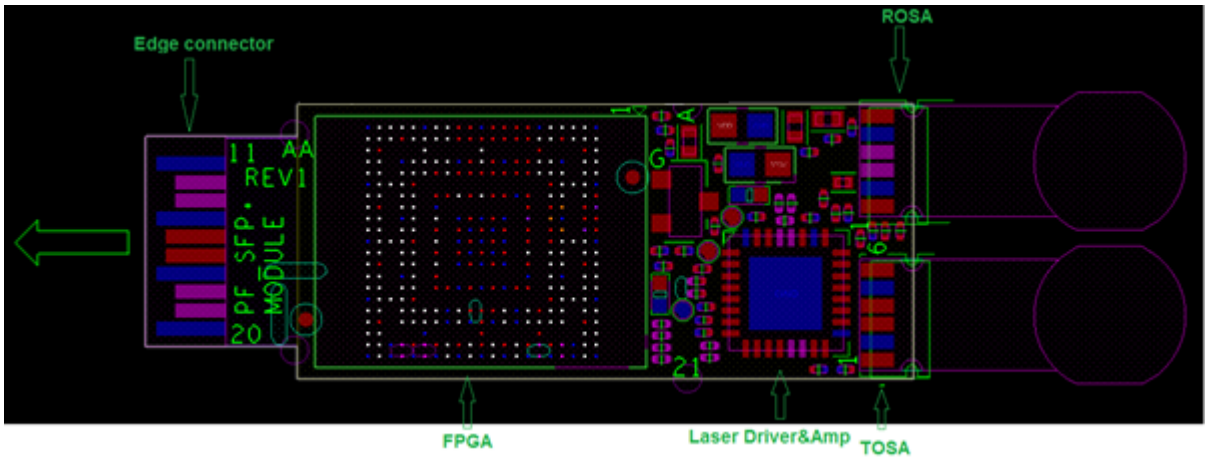
4.1 Hardware Placement

This section describes the top and side view of the FPGA placement.

4.1.1 Top Side FPGA Placement

The following figure shows the top view of the FPGA placement.

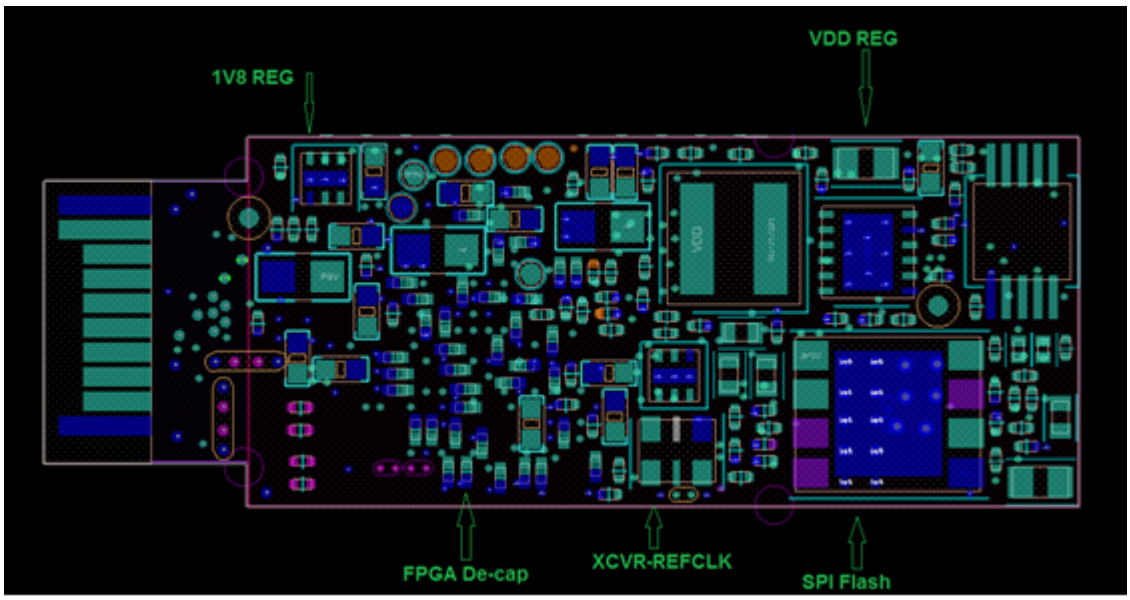
Figure 4-1. FPGA Placement (Top View)



4.1.2 Bottom Side FPGA Placement

The following figure shows the bottom view of the FPGA placement.

Figure 4-2. FPGA Placement (Bottom View)



4.2 Hardware Layout and Design

This chapter briefly describes the PCB layout and material.

4.2.1 Stack Up and Material

The PolarFire SFP+ module is designed with six-layer PCB and Material used is Nelco 4000-13SI.

The stack-up is as follows:

1. Top
2. GND1
3. SIG1
4. Power
5. GND2
6. Bottom

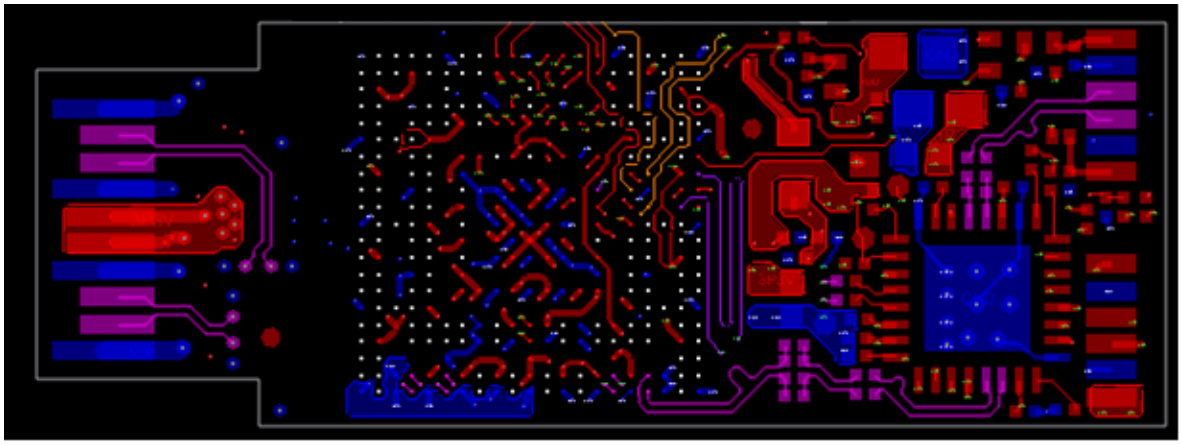
Note: The total PCB thickness is 1 mm with an accuracy of +/- 0.1 mm.

4.2.2 Break-Out Layer By Layer

The Layer-by-Layer break-out is shown in the following figures.

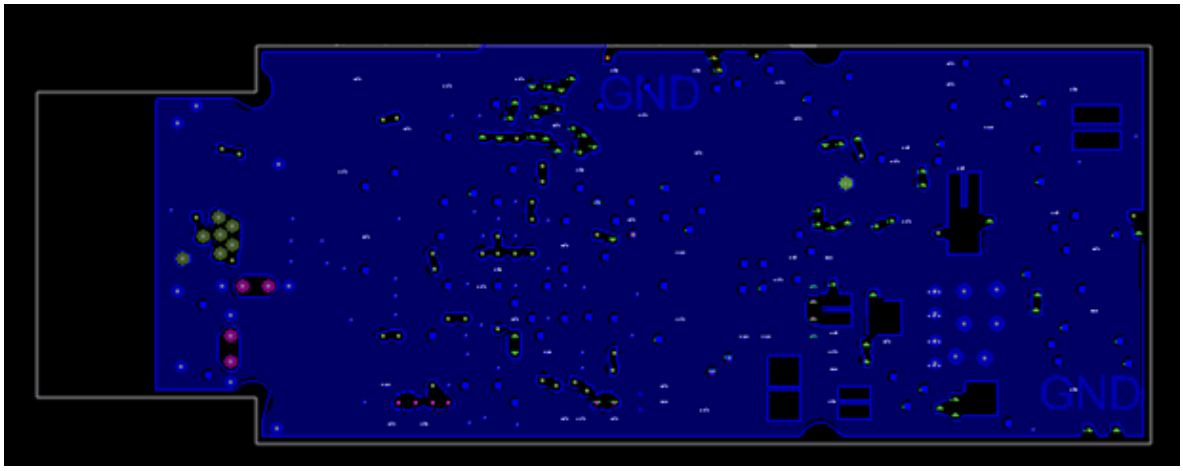
1. The following figure shows the top layer.

Figure 4-3. Top Layer Layout



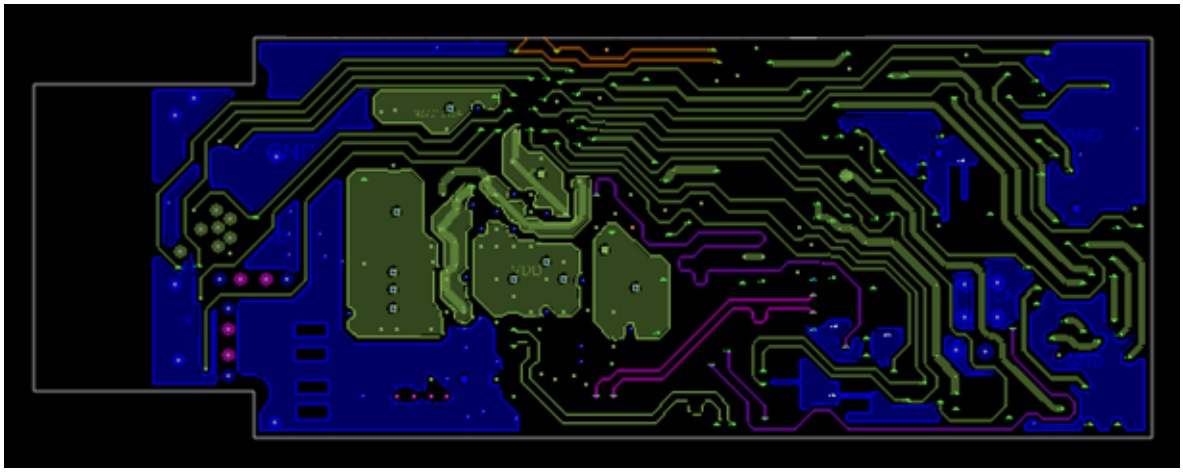
2. The following figure shows the GND1 layer.

Figure 4-4. GND1 Layer Layout



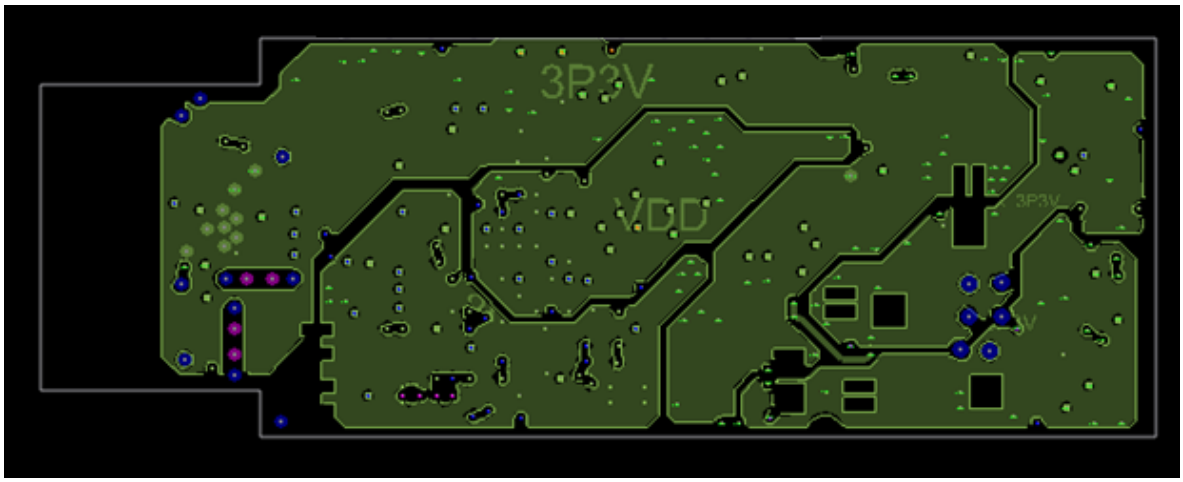
3. The following figure shows the SIG1 layer.

Figure 4-5. SIG1 Layer Layout



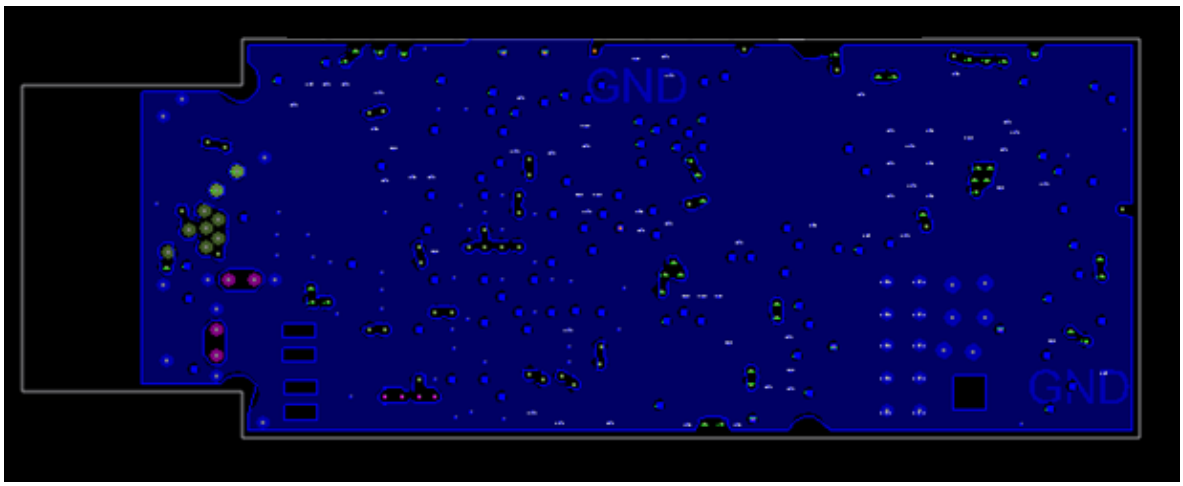
4. The following figure shows the power layer.

Figure 4-6. Power Layer Layout



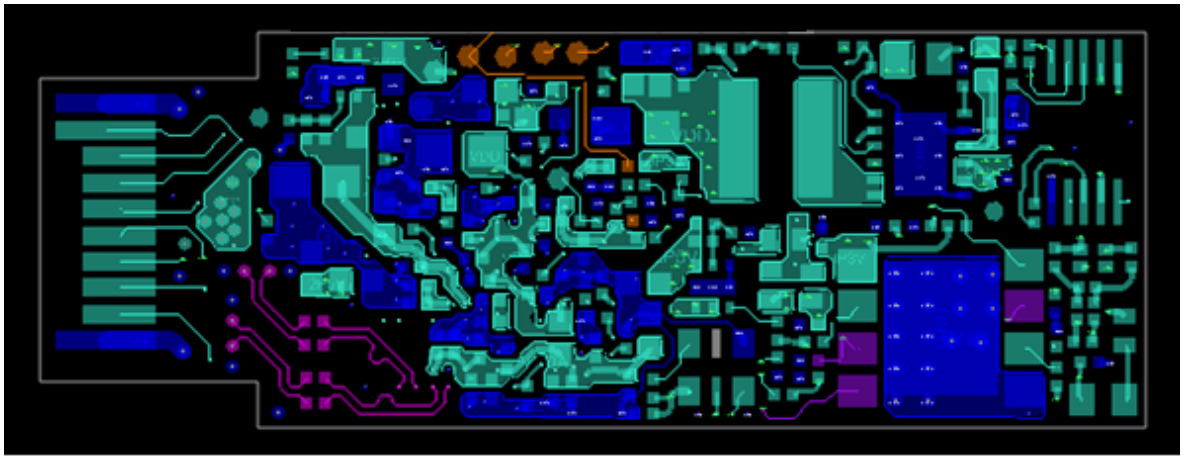
5. The following figure shows the GND2 Layer.

Figure 4-7. GND2 Layer Layout



6. The following figure shows the bottom layer.

Figure 4-8. Bottom Layer Layout



4.3 Power Integrity

The recommended board capacitors are listed in Table 3-1 for the SFP+ application. The bulk capacitors for the VDD mentioned in Table 3-1 are for the PolarFire device only. Table 3-1 does not list the capacitors required for the output of the regulator. The regulator output must follow the capacitor specifications of the regulator vendor.

- The bulk capacitor recommendations for VDD are based on 1.5A of consumption.
- Care must be taken while routing the VDD plane. Ensure that the plane is routed as a dedicated plane so that no IR drop occurs at any location of the net. This would also ensure the ripple for VDD is at a minimum.
- Place all 0.1 µF and 0.01 µF capacitors under device BGA.

Note: For information about the recommended connections for unused power supplies, see Figure 3 and 4 of UG0726: PolarFire FPGA Board Design User Guide.

4.4 Signal Integrity

The following guidelines are recommended for high speed transceiver trace routing.

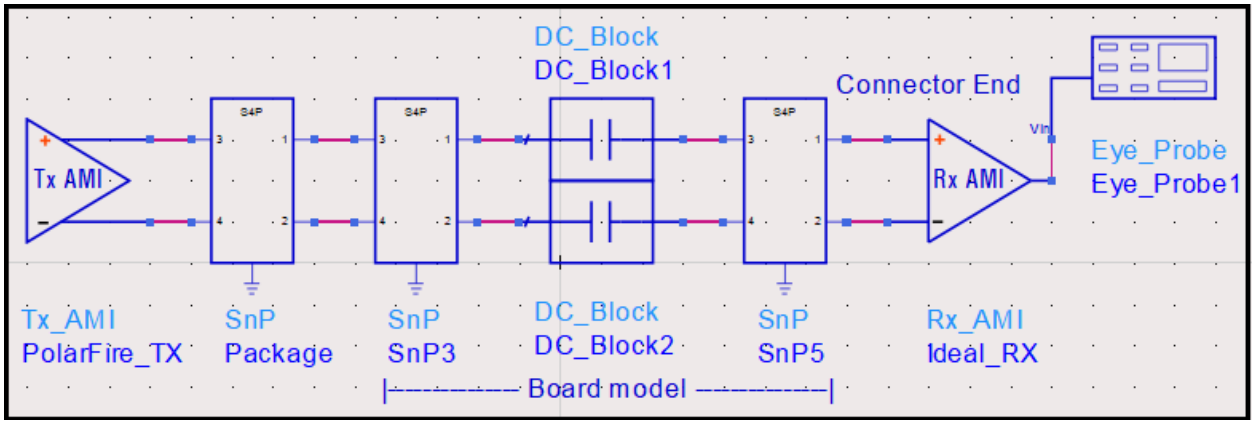
1. Match length between P and N within 1 mil.
2. Maintain the impedance between 85 to 100 ohms.
3. Model the via, BGA pad, and connector discontinuities to match the trace impedance.
4. Use loosely coupled differential traces.
5. Use low loss PCB materials.
6. Use low roughness copper PCB material.

For more information about the routing of high-speed signals, see section 4.2 of UG0726: PolarFire FPGA Board Design User Guide.

4.4.1 IBIS-AMI Simulation

IBIS-AMI simulation was performed on one of the traces going from the PolarFire FPGA TX to the SFP male connector. And, the eye diagram was captured at the connector. The simulation topology is shown in the following figure.

Figure 4-9. IBIS-AMI Simulation Topology



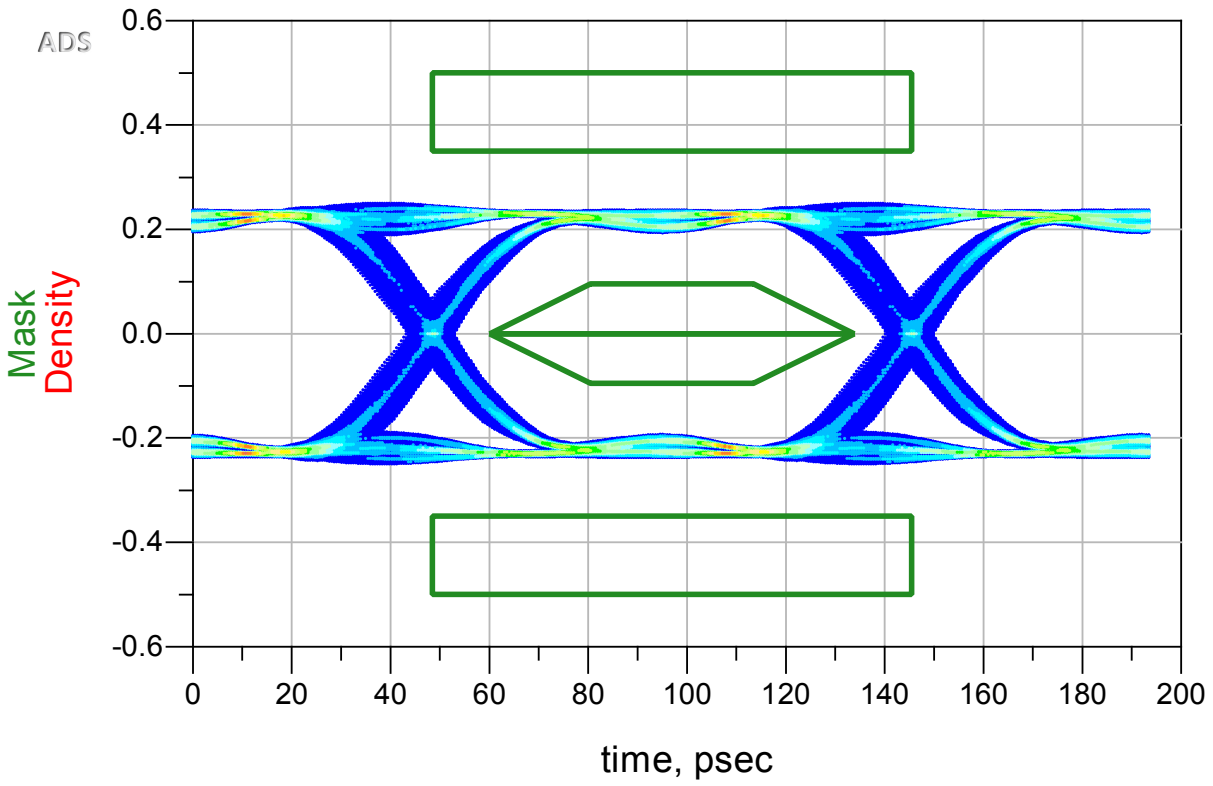
Note: The IBIS-AMI models are available at www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-polarfire.

The simulations parameters for IBIS-AMI are as follows:

- TX amplitude: 400 mV
- De-emphasis: 0 dB
- Driver impedance: 100 ohms

The following figure shows the eye diagram, which included the SFP compliant eye mask. The eye diagram passes the SFP eye mask specification in the simulation. The eye diagram indicates that the trace is optimized for all discontinuities.

Figure 4-10. Eye Diagram



5. Compliance Measurements

This chapter describes the 10GBASE-SR compliance measurements.

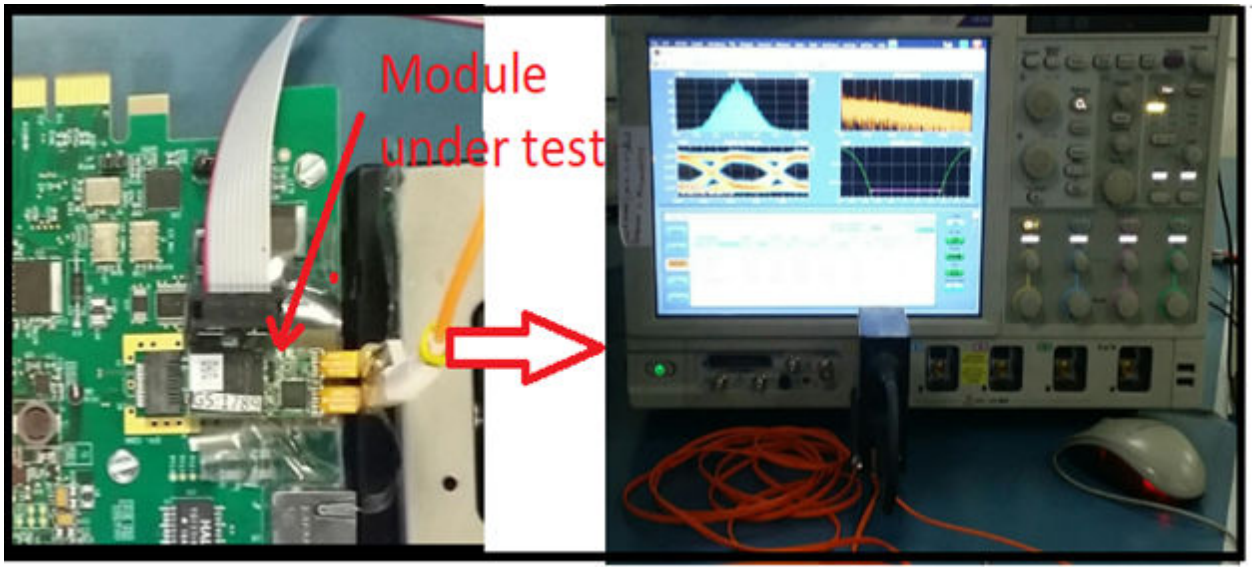
5.1 Set up Details

The following equipments were used.

- Tektronix - Scope MSO72304DX
- Optical probes - DPO7OE1
- Optical cable

The following figure shows the test setup.

Figure 5-1. Test Setup



5.2 Compliance Data

The following table lists different parameters captured during the SFP+ module optical eye testing.

Table 5-1. Parameters for Optical Eye Testing

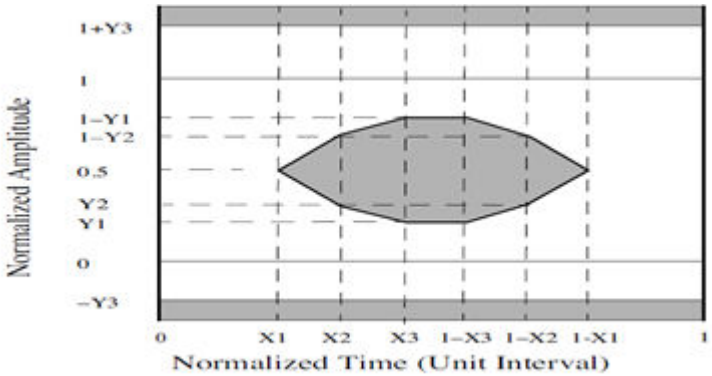
Description	Measured Data	10G BASE- SR Standard	Unit
Signaling speed	10.3125	10.312	Gbps
Wavelength (range)	840-860	840-860	nm
Average launch power (minimum)	–3.17	–7.3	dBm
Extinction ratio	4.92	3	db
OMA (Optical Modulation amplitude)	–2.29	–2.8 to –3.2	dBm

5.2.1 Transmitter Eye

This defines the minimum eye width and height that must be met for the signal to be transmitted clean and without error.

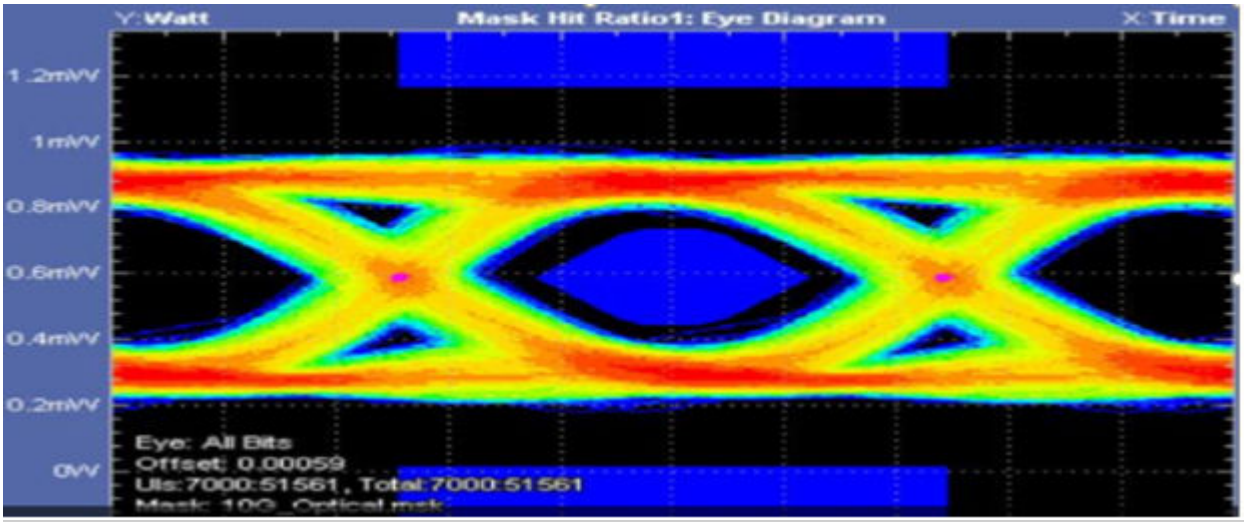
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} {0.25, 0.40, 0.45, 0.25, 0.28, 0.40}

Figure 5-2. Transmitter Eye Mask Definition



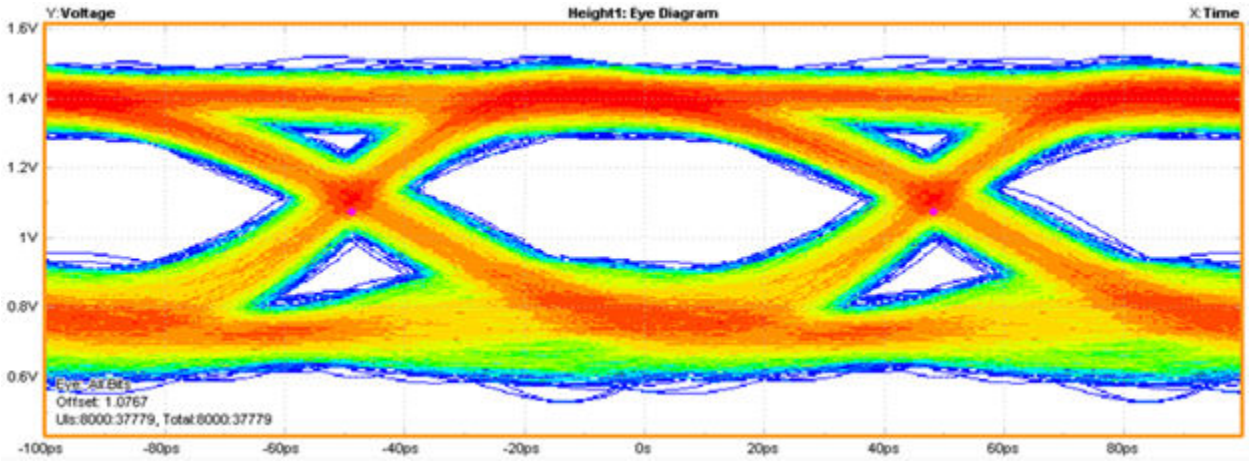
The following figure shows that eye mask parameters were met by the device and a zero hit ratio was observed.

Figure 5-3. Eye Mask Parameters



The following figure shows the optical eye capture with math function added.

Figure 5-4. Optical Eye Capture with Math Function Added



6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	12/2021	This is the intial revision of the document. The following is the summary of the changes in this revision. • Added 5. Compliance Measurements. • Document number was changed from AC480 to AN4364.
1.0	04/2019	This is the first publication of this document (AC480).

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ISBN: 978-1-5224-9521-5

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