



MICROCHIP

QUALIFICATION PLAN SUMMARY

PCN #: MFOL-16YYHO127

**Date:
April 08, 2025**

Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for selected 24LC01B, 24LC04B, 24C02C, 25LC640, 25AA640, 25LC320, 25C320, 25AA320, 24LC64, 24LC02B, 24AA64, HCS101, HCS201, and CHARM2 device families of 121K technology available in various packages.



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Package Qualification Plan

Purpose: Qualification of Microchip Technology Gresham – Fab 4 (GRTM) as a new fabrication location for selected 24LC01B, 24LC04B, 24C02C, 25LC640, 25AA640, 25LC320, 25C320, 25AA320, 24LC64, 24LC02B, 24AA64, HCS101, HCS201, and CHARM2 device families of 121K technology available in various packages. This is a Q100 Grade 1 qualification.

CCB No. 7413.012 and 7364.037

Misc.	Assembly site	MTAI
	BD Number	A-074131
	MP Code (MPC)	B5AB24C2XA04
	Part Number (CPN)	25LC640-E/SN
	MSL information	1
	Assembly Shipping Media (T/R, Tube/Tray)	Tube / T&R
	Base Quantity Multiple (BQM)	100 / 3300
	Reliability Site	MTAI
Lead-Frame	Paddle size	95 x 130 mils
	Material	CDA194
	DAP Surface Prep	Bare Cu
	Treatment	Roughened
	Process	Etched
	Lead-lock <i>(Locking Hole, Half Etched, Dimple, etc. If none, please put No or N/A)</i>	Yes
	Part Number	10100842
	Lead Plating	Matte tin
	Strip Size	MTAI standard
	Strip Density	MTAI standard
Bond Wire	Material	CuPdAu
Die Attach	Part Number	8390A
	Conductive	Yes
MC	Part Number	G600V
PKG	Package Type	SOIC
	Pin/Ball Count	8
	PKG width/size	150 mils

Test Name	Conditions	Reliability Stress Read Point Grade 1: -40°C to +125°C (MCHP E Temp)	Pre & Post Reliability Stress Test Temperature Grade 1: -40°C to +125°C (MCHP E Temp)	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	J-STD-002D; Perform 8 hours of steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.			22	5	1	27	>95% lead coverage	5	Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability- SMD reflow soldering) is required for any plating-related changes and highly recommended for other package BOM changes.
Wire Bond Pull - WBP	Mil. Std. 883-2011			5	0	1	5	0 fails after TC	5	30 bonds from a min. 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001			5	0	1	5	0	5	30 bonds from a min. 5 devices.
Physical Dimensions	Measure per JESD22 B100 and B108			10	0	3	30	0	5	
External Visual	Mil. Std. 883-2009/2010			All devices prior to submission for qualification testing	0	3	ALL	0	5	
HTSL (High Temp Storage Life)	JESD22-A103 +125°C, +150°C or +175°C 2x stress	<u>1st Readpoint:</u> Grade 1: 500 hrs (+175°C) <u>2nd Readpoint:</u> Grade 1: 1000 hrs (+175°C)	Grade 1: +25°C, +85°C, +125°C	45	5	3	150	0	21 - 167	Perform per the requirements in AEC-Q100/Q101. Spares should be properly identified.
Preconditioning - Required for surface mount devices	J-STD-020 JESD22-A113 +150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020E for package type. MSL 1 @ 260 C		Grade 1: +25°C	231	15	3	738	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, uHAST, Temp Cycle test.



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Process Qualification Plan

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CCB No. 7364.037

Test	Number of Lot/s	Sample Size (Per lot)	Total Sample	Conditions
ELFR	3	800	2400	48 hours @ 125°C
DLT	3	77	231	1000 Hours @ 125°C
Retention Bake	3	231	693	1008 hours @ 150°C
ESD (HBM)	1	12	12	±250V, ±500V, ±1KV & ±2KV
ESD (CDM)	1	9	9	±250V, ±500V, ±750V
Latch Up	1	12	12	6 room, 6 125°C AECQ100-004
Electrical Distribution	3	30	90	Data log parameters at room, hot, and cold temperatures at Vcc min/max and Frequency min/max.