Universal Backplane Management (UBM) White Paper

The SCSI Enclosure Services (SES) standard for SAS and SATA backplane management over Serial GPIO was first introduced in 2003. This specification provided for LED control by the host, and allowed the host to detect the presence of bays and installed drives, as well as the bay numbering scheme. The specification provided activity and drive failure indication, and an appropriate controller could discern device type, bifurcation and speed automatically through the protocol. SGPIO has remained unchanged since 2006. Since that time, many innovations have increased the complexity of backplane management beyond the capability of SES and SGPIO.

The modern storage world now includes multi-lane drives and a third drive protocol, namely NVMe. To ensure the same level of functionality, more intelligent backplanes are required. This need produced the Universal Backplane Management (UBM) standard. Without UBM, implementations involving NVMe will require manual configuration of the controller for each backplane variation. In addition, a system for identifying when a NVMe drive is present, versus a SAS/SATA drive, along with SFF-TA-1001 drives, allows for a trimode bay implementation that efficiently uses the high-speed lanes of the host and reduces cabling costs.

Adoption of the UBM standard enables two key aspects of backplane management:

- Construction of a suite of fully interchangeable backplanes within a server, regardless of variations in the backplane interface to the host, or the media supported by the backplane. The use of UBM across the various storage architectures is highly desirable and avoids the complexity of manual configuration and the cost of misconfiguration.
- The ability to create a backplane that supports fully interchangeable storage media types within a drive bay, including changing between NVMe and SAS/SATA while a system is in operation.

UBM is defined in the SFF-TA-1005 industry standard and is sponsored by leading server and storage vendors. UBM is enabled in a variety of storage products offered in the market, and through off-the-shelf components and bundled firmware that are available to enable UBM backplanes today.

Contact Microchip for details on how to build your own UBM backplane, including reference designs and other design collateral.

References

SFF SNIA Committee Specifications
SFF-8448, Reference Guide for SAS Sideband Signal Assignments
SFF-8482, Serial Attachment 2X Unshielded Connector
SFF-8485, Specification for Serial GPIO (SGPIO) Bus
SFF-8630, Serial Attachment 4X Unshielded Connector
SFF-8639, Specification for Multifunction 6X Unshielded Connector
SFF-9402, Reference Guide for Multi-Protocol Internal Cables for SAS and/or PCIe
SFF-TA-1001, Universal x4 Link Definition for SFF-8639, Rev 1.0
SFF-TA-1005, Universal Backplane Management (UBM). Rev 1.0
IPMI format for FRU EEPROM

PCI-SIG
PCI Express SFF-8639 Module Specification (Quad PCIe)

Open Compute Project
"SAS/SATA/NVMe Storage", from OCP Summit 2018

Audience

UBM provides tangible benefits for system integrators, server vendors, and end users.

System Integrators

System integrators benefit from a standards-based backplane management system that allows for backplanes to be interchanged in the system without any modification of the host system or other storage management components. Additionally, backplanes that report their configuration to the host eliminate the need for modification of the configuration of the host when the backplane changes. This eliminates the possibility of misconfiguration causing downtime in integration testing and reduced overhead in built-to-order systems. Lastly, the multiplexing of control and status signals over a single interface reduces cabling requirements from the backplane to the host.

Server Vendors and End Users

The ability of UBM to detect and report the drive type attached to the backplane enables fully tri-mode (SAS/SATA/NVMe) backplanes. Tri-mode backplanes offer two benefits:

- Server vendors benefit from reduced backplane and cable SKUs by offering tri-mode backplanes.
- End users benefit from the versatility of tri-mode backplanes, which reduces the number of system configurations procured and deployed.

Finally, the adoption of a standards-based approach to backplanes helps the industry reduce costs by allowing multiple vendors to provide interoperable solutions.

How UBM Works

UBM can be used to create SAS/SATA backplanes, NVMe backplanes, or combination backplanes that support all three protocols in a single drive bay. As well, the UBM specification can be used in backplanes with SAS/SATA expanders and PCIe switches.

UBM enables the UBM-enabled host (such as CPU, RAID or HBA card, or other storage controller) to know precisely the backplane's capabilities, as well as sense drive type and presence.

UBM Components

The components of a UBM system consist of a FRU and UBM controller, which are connected to the host via a 2-wire interface.

UBM System
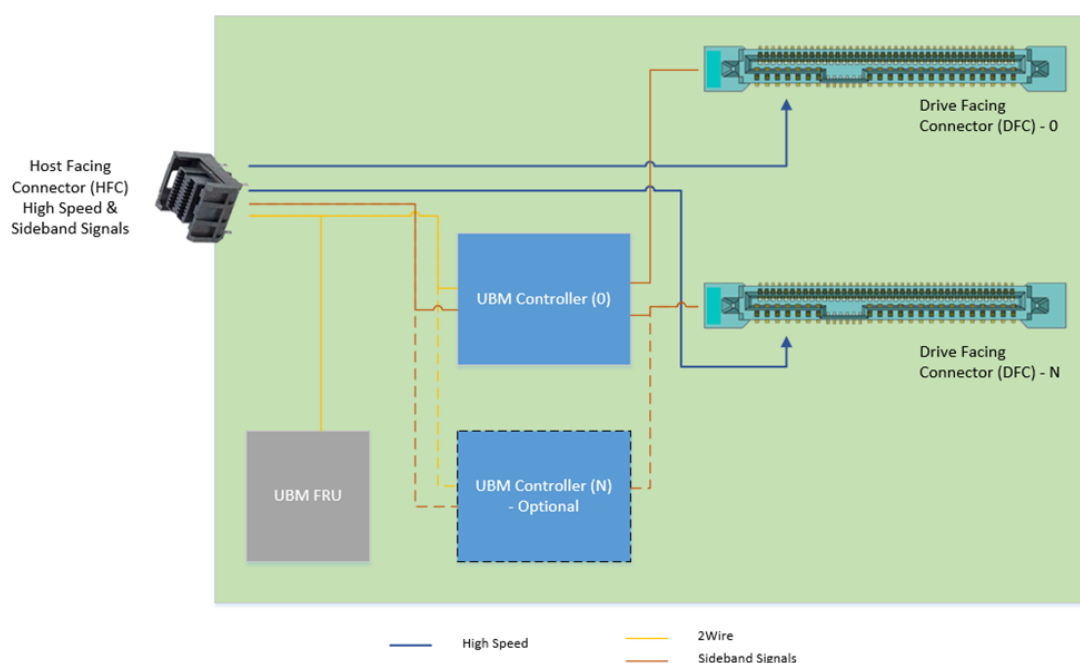
- 2-wire interface
  - UBM uses the sideband signals defined in SAS and other standards in 2-wire mode.
- UBM FRU
  - Provides the means to identify the backplane as a UBM capable subsystem, and is connected to the host via the 2-wire interface.
  - FRU defines the configuration of the backplane.
    - Defines the Port Route Information Descriptors that are used by the host to create an access map consisting of the Drive Facing Connector (DFC), port link width, Host Facing Connector (HFC), and HFC starting lane.
    - Specifies the 2-wire addresses of the UBM controllers connected to the HFC, allowing access by the storage controller.

- UBM controller

  - Responsible for managing the Drive Facing Connectors (DFCs).
  - Accepts pre-determined command sequences via 2-wire that can be grouped into the following categories:

    - Controller Status and Identity: Reports command and controller status.
    - Backplane Capabilities: Reflect the features supported by the UBM controller implementation.
    - Drive Facing Connector Status: The key functionality that allows the UBM Controller to report "What's installed" in each of the drive-facing connectors.

  - Defines PCIe reference clock expectations, PCIe reset expectations, PwrDIS signal support, and dual-port support.
  - The FRU may also contain board or product information areas, within the NVRAM size limit.

UBM Operation

Drive Detection

Drive type identification is performed by sampling the PRSNT#, IFDET#, and IFDET2# pins from the drives. The values of these pins are reported to the host with the DFC Status and Control Descriptor Command. The drive pin states, used in conjunction with the backplane mapping data, allows the appropriate configuration to be applied to the storage controller PHYs connected to that drive.

Bifurcation Port

A backplane wired to support x4 or x2 connections from the Host Facing Connectors to the Drive Facing Connectors can be re-purposed as a x2 or x1 backplane respectively. This is done using the Bifurcation Port field. When the cable attached from the host to the backplane is no longer directly mapped, but routes only one have of the links per drive, the backplane will operate with the DFCs' width divided in two.

By using the Bifurcation Port field, a single backplane can be used in two configurations, reducing the number of backplane SKUs required.

LED and Power Control

LED and power control is performed using the SES Array Device Element field, similar to SAS expanders. The host can request the following actions via the 2-wire interface of the UBM controller:

- Disable power
- Light IDENTIFY LED
- Show "Rebuild" LED pattern
- Show "Failed Array" LED

The LED flash patterns are outside the scope of the UBM specification, but can follow the IBPI specification SFF-8489 corresponding to the condition being signaled by the host interfacing to the UBM controller.

Reset, REFCLK Control

The FRU defines how status and control signals interface between the backplane and the host by defining:

- PCIe reference clock expectations
- PCIe reset expectations
- PwrDIS signal support
- Dual port support (if applicable)

SGPIO Support Through BP_TYPE

The BP_TYPE signal indicates whether the backplane supports SGPIO or 2-wire interface. Using the state of the signal, the host can determine if it should use SGPIO or proceed with UBM discovery.

Maintenance

The UBM specification allows for controller code updates through the UBM Controller Image Update process.
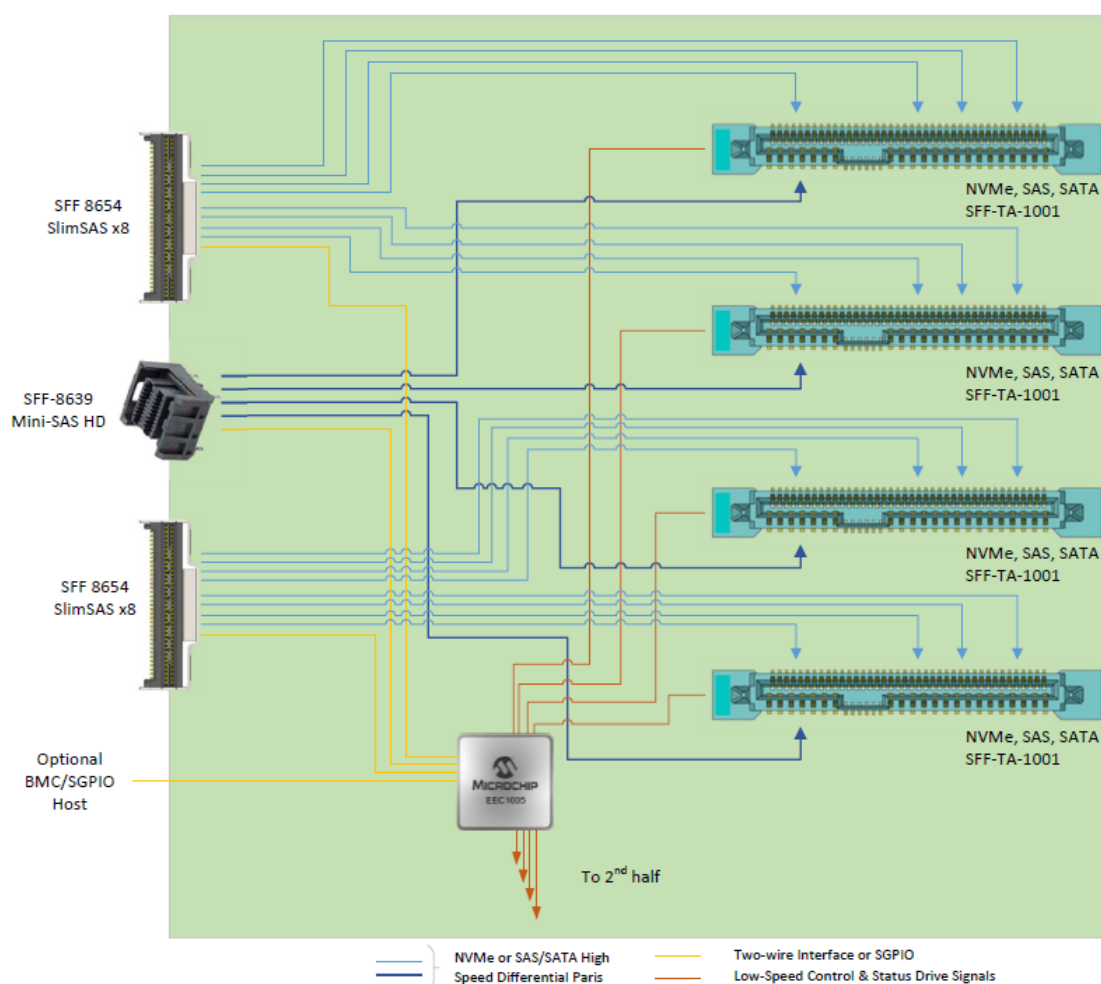
Example UBM Implementations

U.2 and SAS/SATA Backplane

The following illustration shows half of an 8-drive tri-mode backplane capable of supporting x4/x2/x1 U.2 NVMe drives, SAS, or SATA drives. The single UBM controller connects to the host via the sidebands of the SlimSAS and Mini-SAS HD. A subset of this backplane could be used for either SAS/SATA-only or NVMe-only implementations.

- Supports U.2 NVMe and SAS/SATA directly connected to the host or storage controller.
- Each host facing connector supports two x4/x2/x1 U.2 NVMe drives, or 4 x1 SAS/SATA drives.
- UBM controller is placed on the backplane and manages the control and status signals from the drives.

**U.2 and SAS/SATA Backplane**

U.3 and SAS/SATA Backplane

The following illustration shows half of an 8-drive tri-mode backplane capable of supporting x4/x2/x1 U.2 NVMe drives, SAS, or SATA drives. The single UBM controller connects to the host via the sidebands of the SlimSAS and Mini-SAS HD.

- Supports U.3 NVMe and SAS/SATA directly connected to the host or storage controller.
- Each host-facing connector supports two x4/x2/x1 SFF-TA-1001 NVMe/SAS/SATA drives.
- UBM controller is placed on the backplane and manages the control and status signals from the drives.

SFF-TA-1001 NVMe and SAS/SATA Backplane
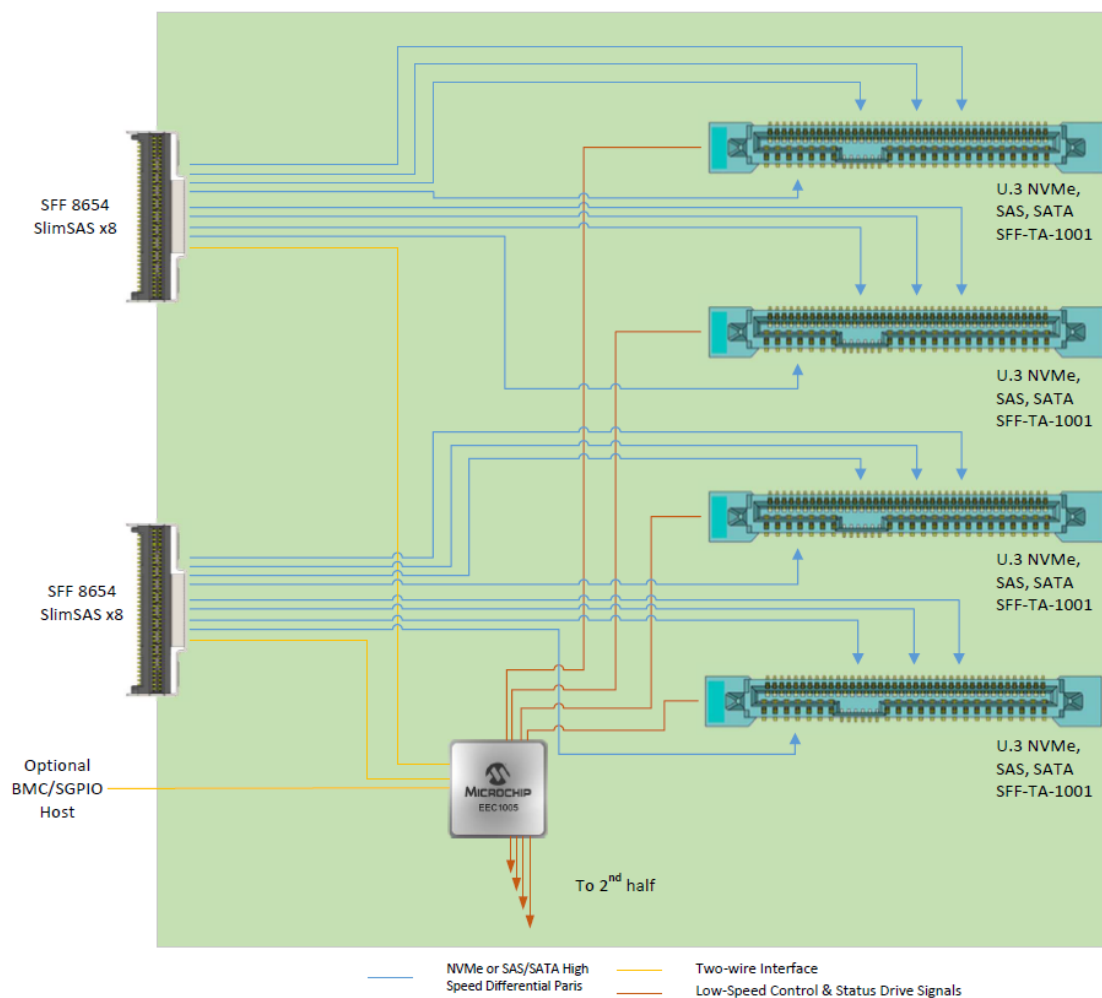
UBM-Enabled Products from Microchip

Microchip is a market leader in UBM solutions.

The SmartRAID 3100, SmartHBA 2100, HBA 1100 SAS/SATA adapters, SmartRAID 3200, SmartHBA 2200, HBA 1200 Tri-Mode adapters, and the Switchtec PFX/PSX/PAX Gen4 PCIe switches[1] from Microchip support UBM, and previous SAS/SATA products are compatible with SmartRAID and SmartHBA adapters through legacy SGPIO support.

Microchip provides UBM FRU/controller solutions through a single microcontroller with fully developed and integration-tested UBM firmware implementation.

Microchip EEC1005 includes:

- ARM Cortex M4 core
- 4 MBit flash, 256KB SRAM, and Kb OTP
- Secure boot and hardware crypto authentication
- Supports backup firmware image
- 16 drive support with four hardware accelerated serial GPIO (SGPIO)
- Universal backplane management integration
- 5 2-wire/SMBus master and slave controllers
- 3 2-wire/SMBus slave controllers
- Scalable for 1–16 drive backplanes
- Cascade solution for more than 16 drives
- 84/144 WFBGA packages

[1] This is a firmware roadmap item.

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