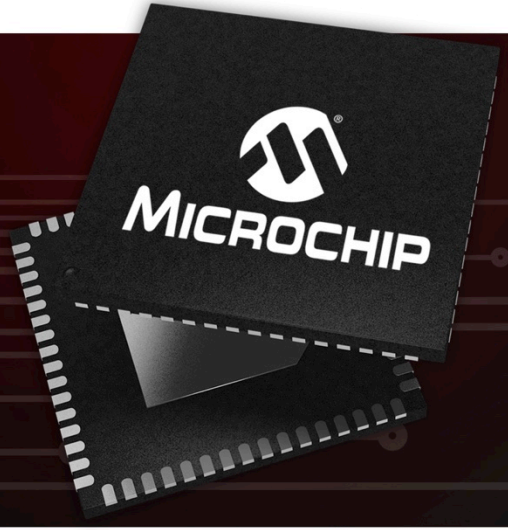
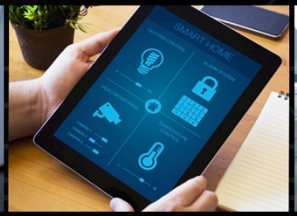
MICROCHIP



A Leading Provider of Microcontroller, Security, Mixed-Signal, Analog & Flash-IP Solutions






Vectron Space Qualified Oscillator Platforms
Scott Murphy, Product Line Manager
Space Forum 2019

Eliminate the Need for SCD Creation

Use Vectron Hi-Rel Standards

✓ Customer Benefits

- No OEM SCD or custom part numbers required
- Ordering codes define EEE pedigree and QA level
- **MIL-PRF-55310/38534 equivalent screening options**
- Clearly defines radiation tolerance of active devices
- Multiple package, output and supply voltage options
- No additional platform qualification required
- Shorter leadtimes and lower overall cost

✓ Supplier Benefits

- Promotes design efficiencies (BOM creation and entry)
- Enables use of standard build documentation
- Encourages hi-rel process consistency
- Procurement and manufacturing economies of scale
- **Revisions posted "real time" to Vectron website**
- Quick design-in capability utilizing overage

OS-68338, Rev O
Hybrid Clock Hi-Rel Standard, ACMOS and TTL Output

DOC200103, Rev H and **DOC207139, Rev B**
Hybrid TCXO Hi-Rel Standard, CMOS/Sinewave or LVDS Output

DOC203679, Rev F (prelim) and **DOC203810, Rev E**
Hybrid Clock Hi-Rel Standard, LVDS or LVPECL Output

DOC204898, Rev D and **DOC204899, Rev D**
Hybrid VCXO Hi-Rel Standard, LVPECL or LVDS Output

DOC204900, Rev E
Hybrid Clock Hi-Rel Standard, High Frequency ACMOS Output

DOC206218, Rev C
Hybrid VCXO Hi-Rel Standard, ACMOS Output, 9x14mm J-lead

DOC206379, Rev B and **DOC206903, Rev B**
300 krad Hybrid Clock Hi-Rel Standard, ACMOS and LVDS Output

DOC206559, Rev C and **DOC206906, Rev C**
Hybrid VCSO Hi-Rel Standard, Sinewave or LVPECL Output

DOC207753, Rev A
Hybrid VCXO Hi-Rel Standard, High Frequency Sinewave Output

Model Number Assignment

Model Prefix	Hi-Rel Standard	Type	Output	Max Freq	Radiation Tolerance
11xx	OS-68338	Clock	ACMOS/TTL	100 MHz	100krad (Si) TID
12xx	DOC203679	Clock	LVDS	200 MHz	100krad (Si) TID
13xx	DOC203810	Clock	LVPECL	700 MHz	50krad (Si) ELDRS
14xx	DOC204900	Clock	ACMOS	160 MHz	100krad (Si) TID
15xx	DOC206379	Clock	ACMOS	100 MHz	300krad (Si) TID
16xx	DOC206903	Clock	LVDS	200 MHz	300krad (Si) TID
21xx/22xx	DOC200103	TCXO	ACMOS/SINE	500 MHz	100krad (Si) TID
2x23/2x33	DOC207139	TCXO	LVDS	200 MHz	100krad (Si) TID
5116	DOC206218	VCXO	ACMOS	100 MHz	100krad (Si) TID
51xx/52xx	DOC207753	VCXO	ACMOS/SINE	675 MHz	100krad (Si) TID
52xx	DOC204899	VCXO	LVDS	200 MHz	100krad (Si) TID
53xx	DOC204898	VCXO	LVPECL	700 MHz	50krad (Si) ELDRS
63xx	DOC206906	VCSO	LVPECL	1.0 GHz	50krad (Si) ELDRS
65xx	DOC206559	VCSO	SINE	1.5 GHz	300krad (Si) TID
EX-219	Catalog Datasheet	EMXO	HCMOS/SINE	120 MHz	100krad (Si) TID
OX-249	Catalog Datasheet	OCXO	ACMOS/SINE/LVDS	100 MHz	300krad (Si) TID

Catalog Part Number Breakdown

1104 R 10M00000 A F

- Model # (Table 1)
- Design Pedigree
  - E = Enhanced Element Evaluation, 100krad Class S die, Swept Quartz
  - R = 100krad Class S die, Swept Quartz
  - V = 100krad Class S die, Non-Swept Quartz
  - X = Class S die, Non-Swept Quartz
  - B = Class B die, Swept Quartz
  - C = Class B die, Non-Swept Quartz
  - D = Ruggedized COTS: Commercial Grade Components, Non-Swept Quartz
- Frequency
- Input Voltage
  - A= +5.0V
  - B= +3.3V
- Screening Option per Table 5, 5.1.1

CLOCK
VCXO
VCSO

TCXO

2101 R 100M0000 E B S

- Model # (Table 1)
- Design Pedigree
  - E = Class S Components, Enhanced Element Evaluation Swept Quartz
  - R = Class S Components, Swept Quartz
  - B = Class B Components, Swept Quartz
  - C = Class B Components, Non-Swept Quartz
  - D = Ruggedized COTS: Non-Swept Quartz, Commercial Grade Components
- Temperature Stability
  - A = ±0.5ppm, 0°C to +50°C
  - B = ±1ppm, 0°C to +50°C
  - D = ±1ppm, 0°C to +70°C
  - F = ±2ppm, 0°C to +70°C
  - I = ±5ppm, 0°C to +70°C
  - K = ±1ppm, -20°C to +70°C
  - M = ±2ppm, -20°C to +70°C
  - R = ±5ppm, -20°C to +70°C
  - T = ±2ppm, -40°C to +85°C
  - V = ±4ppm, -40°C to +85°C
  - W = ±5ppm, -40°C to +85°C
  - Y = ±10ppm, -55°C to +105°C
- Input Voltage
  - A = +3.3V
  - B = +5V
  - C = +12V
  - D = +15V
- Screening Option per Table 4, 5.1.1

Release of MIL-PRF-55310, Rev F

❑ Device Screening Changes [Product Level S Class 2 (Hybrid) Crystal Oscillators]

- Temp cycle test condition change from B to C
- PIND test condition change from B to A
- Seal tests (fine/gross) now mandate MIL-STD-883, Method 1014 (Kr-85 mandate for gross leak test)
- Additional delta limit considerations apply to burn-in

❑ Group C Inspection Changes [Product Level S Class 2 (Hybrid) Crystal Oscillators]

- Random vibration test added to SG1
- Seal tests must also comply with MIL-STD-883, Method 1014 requirements
- Life test (1,000 hours @ +125C) added as SG5 on 25% of test specimens

❑ Vectron Response

- All fourteen hi-rel standards were recently revised (April 2019) in order to add a new screening code which reflects **full compliance with Revision F** Screening and Group C requirements for Product Level S devices

Clock/VCXO/VCSO Screening Options (REVISED)

OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option S	Option X
	SCREENING	**MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)**	K 100%	B- 100%	S- 100%	K+ 100%	B 100%	S (Rev E) 100%	100%	**S (Rev F) 100%**	EM 100%
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	NR	X	X	NR	X	NR	**X**	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K, Meth 2032 Class K	X	X	X	X	X	X	X	**X**	X
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.	**X 48 hrs.**	X 24 hrs.
4	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	NR	NR	X	NR	NR	X	NR	**X**	NR
5	**Temperature Cycle**	**MIL-STD-883, Meth 1010, Cond. B (except Option S), 10 cycles min.**	X	X	X	X	X	X	X	**X Cond. C**	NR
6	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	X	X	**X**	NR
7	**Particle Impact Noise Detection**	**MIL-STD-883, Meth 2020, Cond B (except Option S)**	X	X	X	X	X	X	NR	**X Cond. A**	X
8	Electrical Testing, Pre Burn-In	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	X	X	X	X	X	X	**X**	X
9	1st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	**X 240 hrs.**	NR
10	Electrical Testing, Intermediate	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	NR	NR	X	NR	NR	NR	**NR**	NR
11	2nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	**NR**	NR
12	Freq-Temp Slew Test	Operating temp. range, frequency plotted at 1.0°C steps	AR	AR	AR	AR	AR	AR	NR	**AR**	NR
13	Electrical Testing, Post Burn-In (Group A)	Perform tests in Table 3. Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X	X	X	X nom. Vcc	**X**	NR
14	Seal: Fine Leak Seal: Gross Leak	MIL-STD-202, Meth 112, Cond C (5×10^{-8} atm cc/sec max) MIL-STD-202, Meth 112, Cond D	X	X	X	X	X	X	X	**NR**	X
15	**Seal: Fine Leak Seal: Gross Leak**	**MIL-STD-883, Meth 1014, Cond A2 or B1 MIL-STD-883, Meth 1014, Cond B2 or B3**	NR	NR	NR	NR	NR	NR	NR	**X**	NR
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	AR	AR	X	AR	X	NR	**X**	NR
17	Solderability	MIL-STD-883, Meth 2003	1/	1/	1/	1/	1/	1/	1/	**1/**	NR
18	External Visual & Mechanical	MIL-STD-883, Meth 2009	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	X 2/	**X 2/**	X 2/
19	Aging, 30 Day 3/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	X	13 pcs.	X	NR	**X**	NR
20	**Group C Inspection (optional)**	**See Para 5.2 herein for details of supplier recommended Group C Inspection options**	**5.2(g)**	**5.2(e)**	**5.2(e)**	**5.2(g)**	**5.2(e)**	**5.2(e)**	**5.2(e)**	**5.2(f)**	**NR**

TCXO
Screening Options (REVISED)

OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option K	Option F	Option S	Option C	Option B	Option X
	SCREENING	**MIL Class Similarity (MIL-PRF-55310, Class S/B or MIL-PRF-38534, Class K)**	M38534K K	**M55310F S**	M55310E S	M55310E B+	M55310E B	EM
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	**X**	X	NR	NR	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K or H, Meth 2032 Class K or H	X K	**X K**	X K	X H	X H	X H
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	**X 48 hrs.**	X 48 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.
4	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	X	**X**	X	NR	NR	NR
5	**Temperature Cycle**	MIL-STD-883, Meth 1010, Cond. B, 10 cycles min.	X	**NR**	X	X	X	NR
		MIL-STD-883, Meth 1010, Cond. C, 10 cycles min.	NR	**X**	NR	NR	NR	NR
6	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	**X**	X	X	X	NR
7	**Particle Impact Noise Detection**	MIL-STD-883, Meth 2020, Cond B	X	**NR**	X	X	NR	NR
		MIL-STD-883, Meth 2020, Cond A	NR	**X**	NR	NR	NR	NR
8	Electrical Testing, Pre Burn-In	Nominal Vcc, +25°C	X	**X**	X	X	X	X
9	1st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	**X 240 hrs.**	X 240 hrs.	X 160 hrs.	X 160 hrs.	NR
10	Electrical Testing, Intermediate	Nominal Vcc, +25°C & Op Temp Extremes	X	**NR**	NR	NR	NR	NR
11	2nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	**NR**	NR	NR	NR	NR
12	Electrical Testing, Post Burn-In	Nominal Vcc & extremes, nominal temperature & extremes	X	**X**	X	X	X	NR
13	**Seal: Fine Leak**	MIL-STD-202, Meth 112, Cond C, 5 x 10^{-8} atm cc/sec max	X	**NR**	X	X	X	X
		Mil-STD-883, Meth. 1014, TC A2 or B1	NR	**X**	NR	NR	NR	NR
14	**Seal: Gross Leak**	MIL-STD-202, Meth 112, Cond D	X	**NR**	X	X	X	X
		MIL-STD-883, Meth. 1014, TC B2 or B3	NR	**X**	NR	NR	NR	NR
15	Radiographic Inspection	MIL-STD-883, Meth 2012	X	**X**	X	X	NR	NR
16	Solderability	MIL-STD-883, Meth 2003	1/	**1/**	1/	1/	1/	1/
17	External Visual Inspection	MIL-STD-883, Method 2009	X	**X**	X	X	X	NR
18	Group A Electrical Test	MIL-PRF-55310	X	**X**	X	Sample	Sample	NR
19	Aging, 30 Day 2/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	X	**X**	X	Sample	Sample	NR
20	**Group C Inspection (optional)**	**See Para 5.2 herein for details of supplier recommended Group C Inspection options**	**Para 5.2(g)**	**Para 5.2(f)**	**Para 5.2(e)**	**Para 5.2(e)**	**Para 5.2(e)**	**NR**

Clocks for Driving RTG4 FPGA

Applications note AN3216 just released September 2019 and located on Vectron Space webpage at *https://www.vectron.com/products/space/AN3216_RTG4_App_Note.pdf*.
The following Vectron space qualified clock oscillators have been characterized and are recommended for use with RTG4 REFCLK receivers:

- **LVDS:**
  - **DOC203679**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, LVDS Output
  - **DOC206903**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, 300 krad Tolerant LVDS
- **LVPECL:**
  - **DOC203810**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, LVPECL Output
- **CMOS:**
  - **OS-68338**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, CMOS Output
  - **DOC206379**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, 300 krad Tolerant CMOS
  - **DOC204900**, Oscillator Specification, Hybrid Clock for Hi-Rel Standard, High Frequency CMOS

RTG4 Clock Applications Note

General Recommendations and Summary

1. When an external resistor like the 200Ω termination for differential driving is used, it must be placed as close as possible to the differential receiver input pins. Otherwise, waveform and jitter would greatly degrade.
2. RTG4 differential receiver must be terminated at the inputs either with an external resistor (100Ω or 200Ω) or with ODT (RTG4 on-die termination) for all clock driver types for best waveform and jitter performance.
3. The clock oscillator driver should be placed as close as possible to the input pins of the RTG4 receiver, to help reduce interferences and minimize reflection on the transmission line due to possible impedance mismatching.
4. It is recommended to use the drivers and interface circuits listed in Table 3. ****Do not use the RTG4 REFCLK Inputs LVDS33 and LVPECL33.**

TABLE 4: RTG4 REFCLK Inputs and Clock Driver Matrix

	RTG4	VECTRON CLOCK DRIVER					
Signal Type	REFCLK Inputs	Clock Type	Vectron Hi-Rel Standard Drawing	Radiation Tolerance (krad)	Supply Voltage (V)	Max Freq (MHz)	Termination Circuit
Differential	LVDS25_ODT	LVDS	DOC203679	100	3.3	200	Direct interface Figure 1
			DOC206903	300	3.3	200	
	LVDS25_ODT	LVPECL	DOC203810	50 (ELDRS)	3.3	700	Figures 6, 8, and 10
	LVDS25	LVDS	DOC203679	100	3.3	200	200 Ohms Figure 3
			DOC206903	300	3.3	200	
	LVDS33	Do not use					
	LVPECL33	Do not use					
Single-Ended	LVCMOS33	CMOS	OS-68338	100	3.3	100	Direct interface Figure 12
			DOC204900	100	3.3	125	
			DOC206379	300	3.3	80	
	LVCMOS25	CMOS	DOC204900	100	2.5	125	Direct interface Figure 12

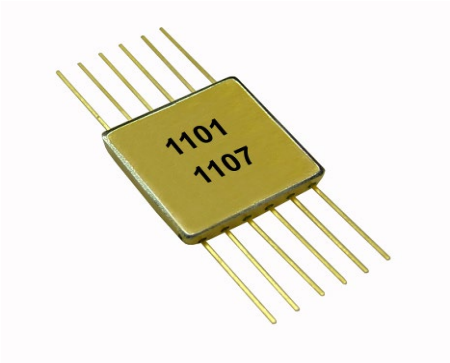
For differential signal application, the only choice for RTG4 to set to is LVDS25_ODT (used with LVDS or LVPECL clock driver) or LVDS25 (used with LVDS clock driver and external 200-ohm termination). The CMOS single-ended signal solution offers the best Total Jitter and Deterministic Jitter performance (See Jitter Measurements Table 5, Table 6 and Table 7), simple direct interface and options to use either the 2.5V or 3.3V supply, but speed is limited to 100MHz (OS-68338), 80MHz (DOC206379) and 125MHz (DOC204900) for the three Vectron CMOS clocks.

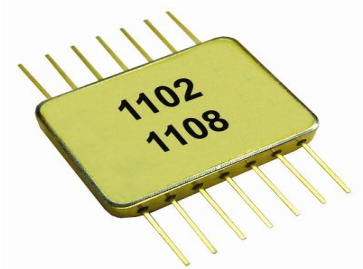
OS-68338, Rev O
(Released April 2019)

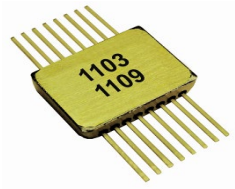
ACMOS/TTL Hi-Rel Clocks

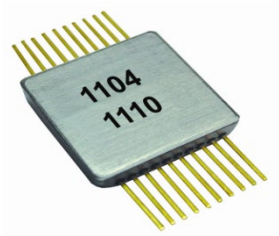
- Addition of three leaded 5x7mm follow-on platforms to legacy Model 1157 (LCC):
  - Model 1167 (straight leads)
  - Model 1177 (gull-winged leads in)
  - Model 1187 (gull-winged leads out)
- Utilizes ruggedized 3-point crystal mount
- All 5x7mm platforms available up to 100 MHz
- Must order separate DPA & RGA destruct specimens on all 5x7mm platforms due to the likelihood of crystal damage
- Now quoting pre-crystal AND post-crystal mount pre-cap inspections if components are mounted under the crystal
- Now offering 20 MP High Resolution Digital Pre-Cap Photos
- All platforms tolerant to 100 krad (Si) TID and characterized to 120 MeV-cm2/mg (SEL) and 40 MeV-cm2/mg (SET)

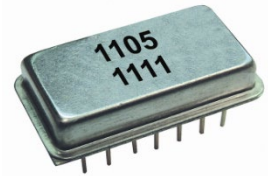
OS-68338 Legacy Enclosures









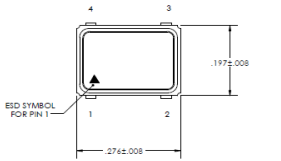


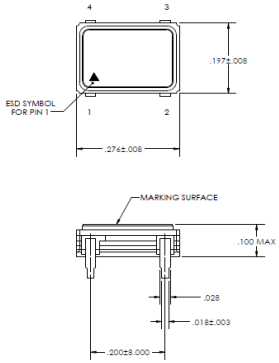
Leaded 5x7mm Clock Family

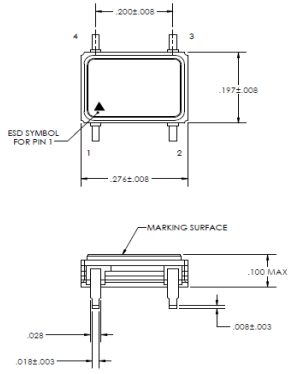
Customers want to know how they can:

- ✓ Minimize clock oscillator footprint
- ✓ Eliminate concerns regarding CTE mismatch between ceramic and board material
- ✓ Reduce the difficulty in solder joint inspection of LCC pads

HI-REL STANDARD MODEL #	PACKAGE	OUTPUT	PIN I/O				MECHANICAL OUTLINE
			Vcc	Out	Gnd/ Case	E/D	
1157	5x7mm 4 pad LCC	ACMOS	4	3	2	1	FIGURE 8
1167	5x7mm Straight Lead	ACMOS	4	3	2	1	FIGURE 13
1177	5x7mm Gull Wing (In)	ACMOS	4	3	2	1	FIGURE 14
1187	5x7mm Gull Wing (Out)	ACMOS	4	3	2	1	FIGURE 15







DOC203679, Rev F
(Prelim Now Posted)

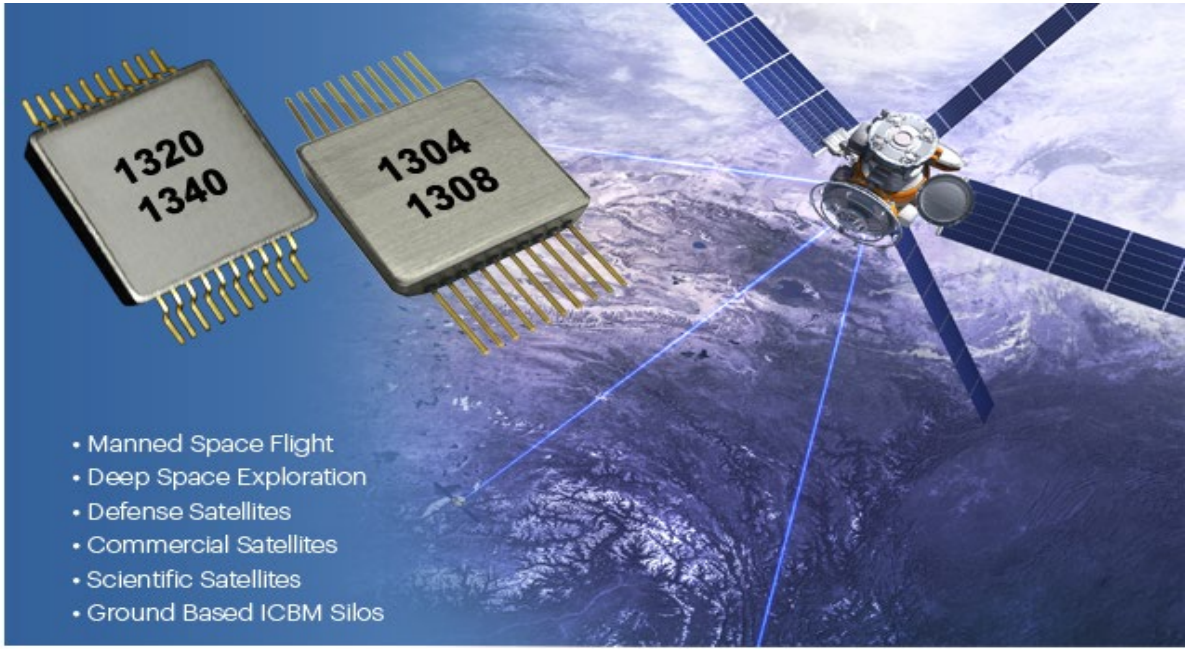
LVDS Hi-Rel Clocks

- Popular for driving rad-tolerant FPGAs such as RTG4, VIRTEX 5QV, et al
- Single, Dual and Quad complementary output pairs available to 200 MHz
- App note AN3216 depicting clock interface circuitry for optimum RTG4 performance released in early September
- Output buffer rated to 1E13 N/cm2 (DDD) and thresholds of 100 MeV-cm2/mg (SEL) and 84.96 MeV-cm2/mg (SET)
- Includes typical jitter and phase noise performance for industry standard frequencies including 100, 125, 156.25 and 200 MHz
- Popular 16x16mm 20FP enclosure w/ optional leadforming
- Revision F (prelim) includes 10x13mm 16FP package option for single complementary output pair (1203/1219)
- Platform qualification expected complete end of November

DOC203810, Rev E
(Released April 2019)

LVPECL Hi-Rel Clocks

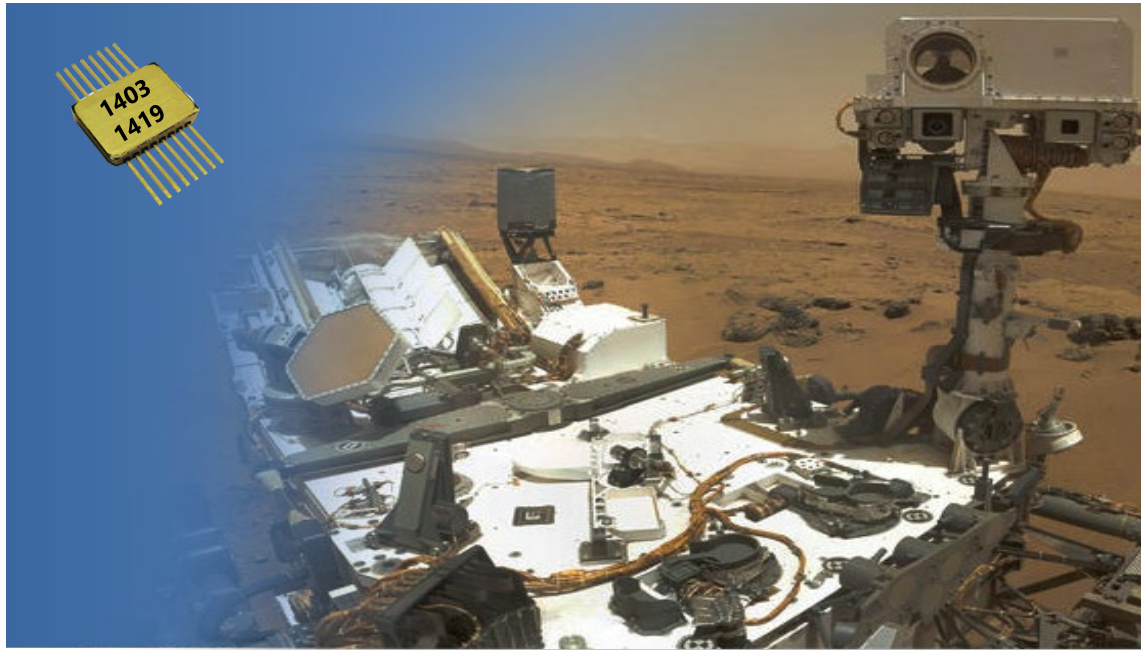
- Popular for driving rad-tolerant FPGAs such as RTG4, VIRTEX 5QV, et al
- Single and dual complementary output pairs available up to 200 MHz in popular 16x16mm 20FP enclosure
- Upper frequency limit expanded to 700 MHz (single pair)
- App note AN3216 depicting clock interface circuitry for optimum RTG4 performance released in early September
- Output buffer guaranteed to 50 krad (Si) ELDRS via wafer lot specific RLAT
- Includes maximum bandwidth limited (12kHz to 20MHz) and period (1 sigma) jitter performance
- Includes optional lead-forming with recommended solder pad layouts
- Added enhanced electrical performance table
- Now includes NASA INST-EEE-002 Level 1 and Level 2 reliability compliance comparisons



DOC204900, Rev E
(Released April 2019)

High Frequency ACMOS Hi-Rel Clocks

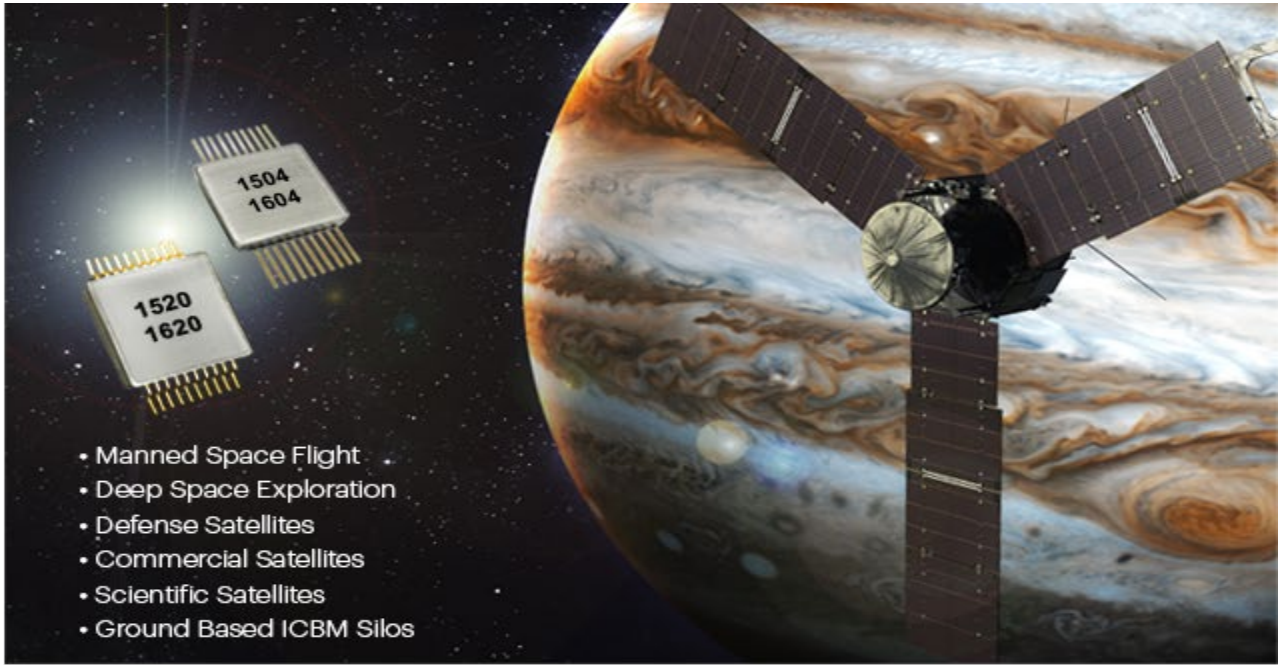
- Transistor-based oscillator available from 12 MHz to 160 MHz
- Utilizes 5962R microcircuit for 100 krad (Si) TID tolerance and SEL/SET/SEU free to >90MeV-cm2/mg
- Now available with +2.5V supply option (low current)
- App note AN3216 depicting clock interface circuitry for optimum RTG4 performance released in early September
- Optimized layout now reduces legacy 16x16mm 20FP offering to a 10x13mm 16FP enclosure:
    - Model 1403 (straight leads)
    - Model 1419 (leadformed)
- Includes leadforming options with recommended pad layouts
- Now includes thermal characteristics, jitter performance and typical phase noise plots



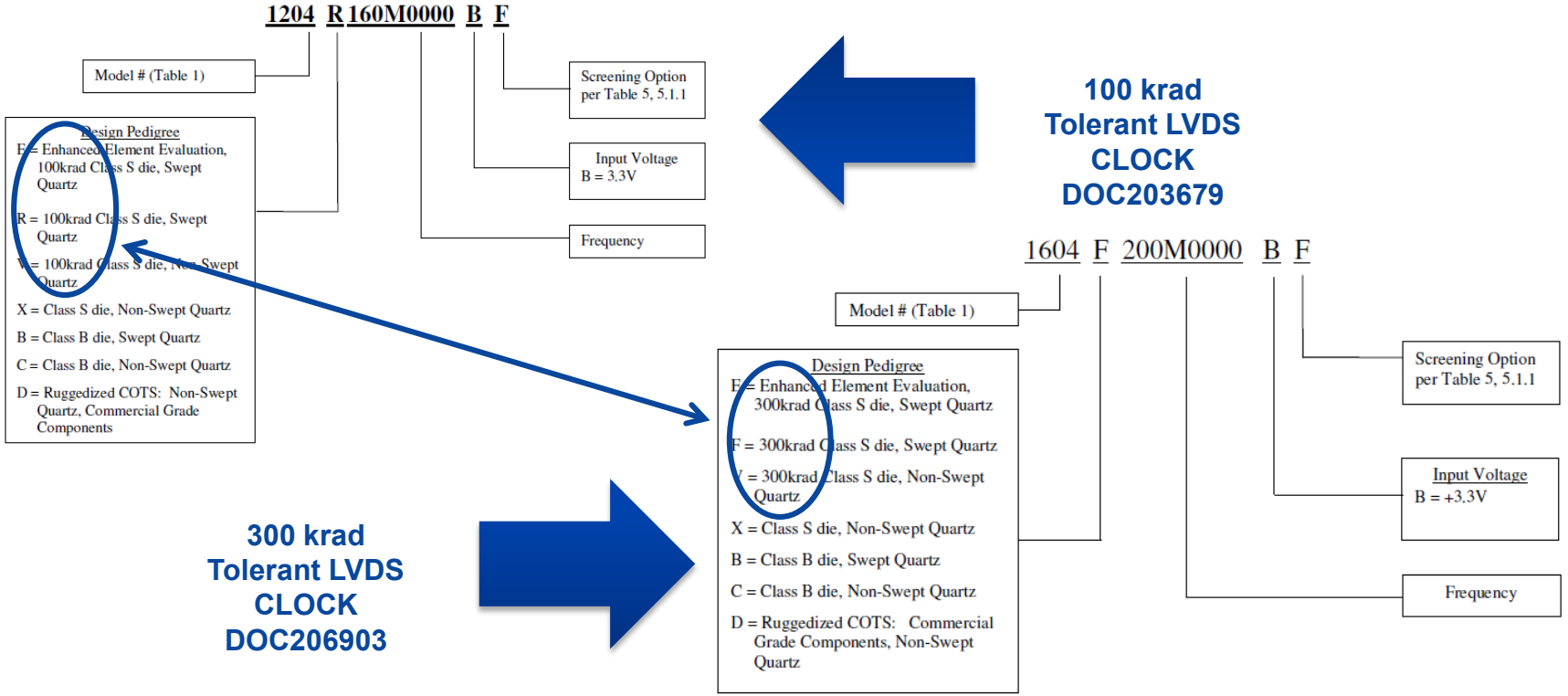
DOC206379 & DOC206903, Rev B
(Released April 2019)

300 krad (Si) Tolerant Hi-Rel Clocks

- Specially designed for deep space missions such as EUROPA and JUICE:
  - ACMOS (DOC206379)
  - LVDS (DOC206903)
- Utilize 5962F microcircuits and high FT bipolar transistors possessing wafer lot specific RLAT
- Active devices guaranteed to have no SEL occurrences at effective LET of ≤93 (ACMOS) and ≤120 (LVDS) MeV-cm2/mg
- Popular 16x16mm 20-lead flatpack enclosure
- Note: For Europa ACMOS clock applications, use JPL 10403039 and JPL 10331716 to capture PETS Class 1 passive device mandates



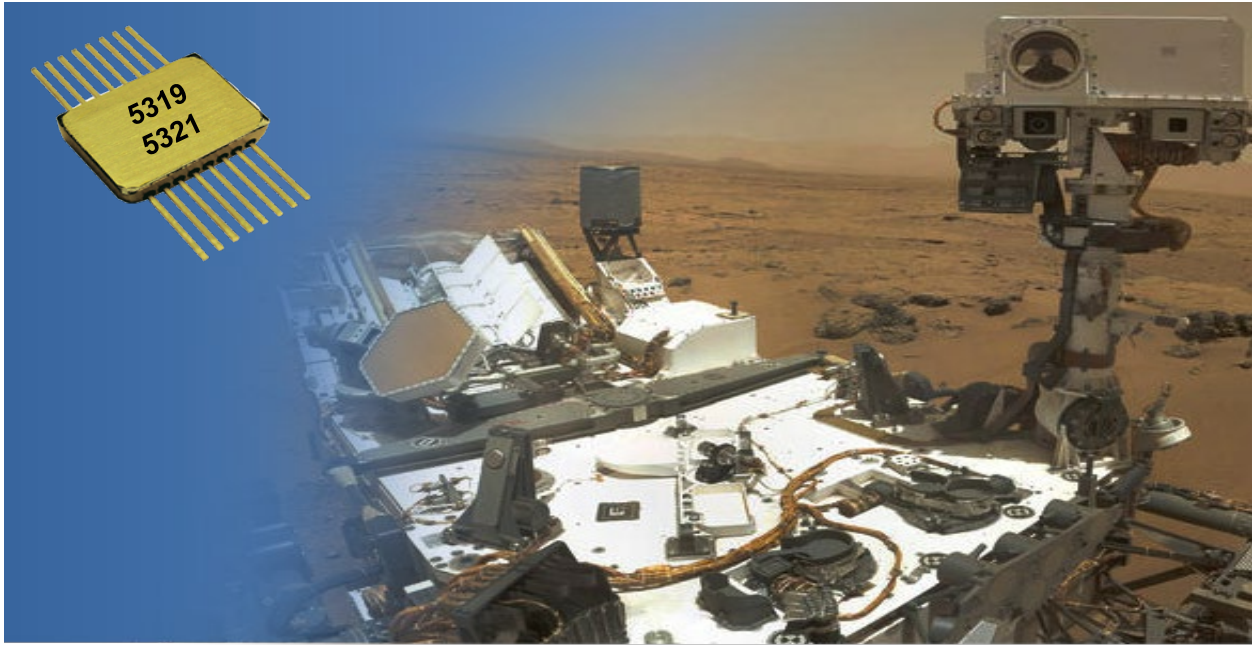
Radiation Tolerance Designation



DOC204898, Rev D
(Released April 2019)

LVPECL Hi-Rel VCXOs

- Popular for driving rad-tolerant Clock Synchronizers and Jitter Cleaners such as CDCM7005-SP, et al
- Nominal frequency upper limit has been extended to 700 MHz
- Robust design utilizes ruggedized 4-point crystal mount
- Output buffer guaranteed to 50 krad (Si) ELDRS via wafer lot specific RLAT
- Minimum Absolute Pull Range (APR) of ±20 ppm
- Maximum Linearity of 10%
- Includes maximum bandwidth limited (12 kHz to 20 MHz) jitter performance
- Includes improved outline drawings, lead-forming options and recommended pad layouts



DOC206559, Rev C
(Released April 2019)

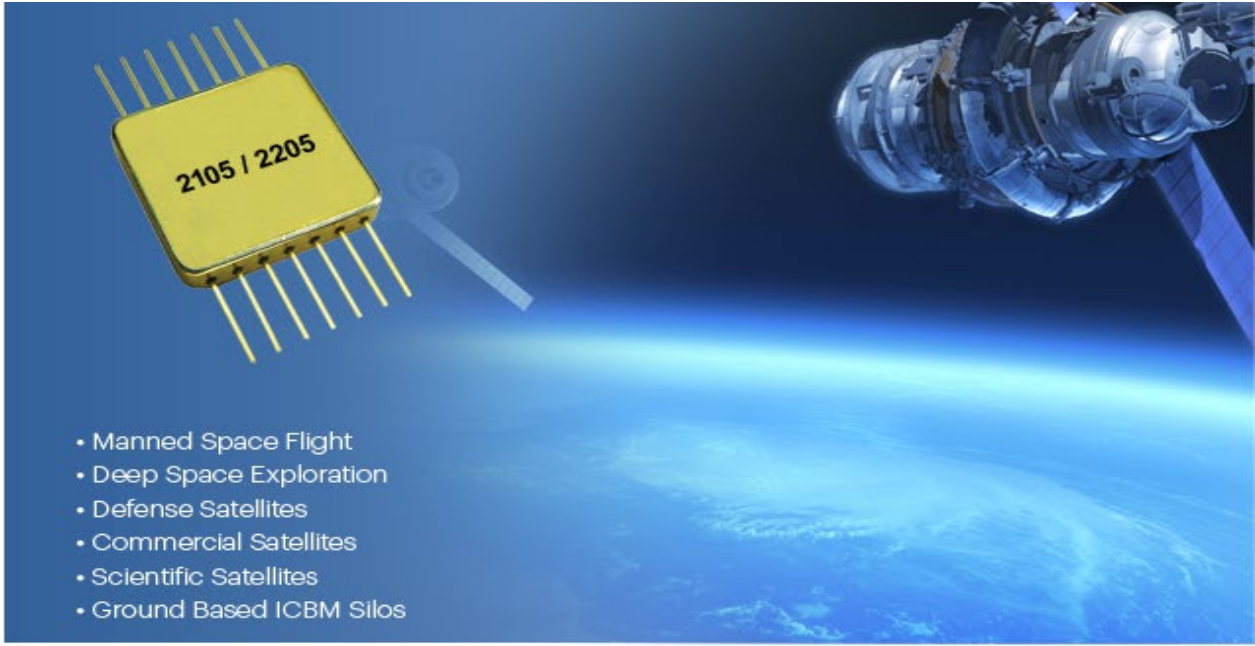
Sinewave Hi-Rel VCSOs

- SINE output available from 300 MHz to 1.5 GHz
- No frequency multiplication promotes better phase noise with no subharmonics
- Includes typical phase noise performance
- Available with 3.3V, 5V or 12V supply options
- Minimum Absolute Pull Range (APR) of ±20 ppm
- Utilizes 300 krad tolerant, SEE insensitive, high FT bipolar transistors w/ wafer lot specific RLAT
- Internal Microchip SAW resonator fab house promotes consistent quality and performance from engineering units to flight hardware
- Popular 16x16mm 20-lead flatpack enclosure
- Optional lead-forming available
- Recommended solder pad layout included

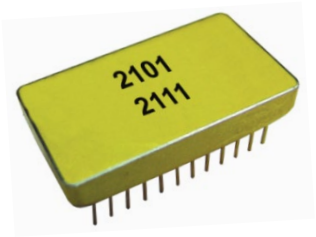
DOC200103, Rev H
(Released April 2019)

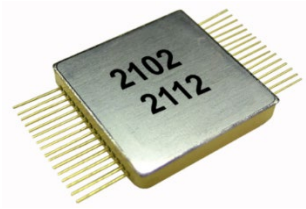
ACMOS/SINE Hi-Rel TCXOs

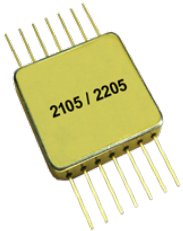
- Smallest fully space qualified, 100 krad (Si) tolerant TCXO available to the industry!!!
- Miniature flat-pack enclosure: 19 x 19 x 6.6 mm
- New model numbers include:
  - ACMOS (2105/2205) up to 100 MHz
  - Sinewave (2115/2215) up to 150 MHz
- Radiation tolerant to 100 krad (Si) TID
- Optional lead-forming now available on all flatpack enclosures
- Recommended solder pad layouts added for all lead-formed devices
- Due to the numerous layout configurations, please consult factory for typical phase noise performance
- All platforms employ tantalum cap filter which eliminates phase noise hump and reduces potential for signal errors due to transients up to 80 MeV

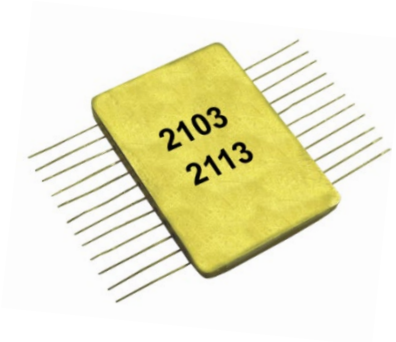


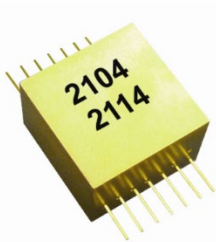
To-Scale Enclosure Comparison











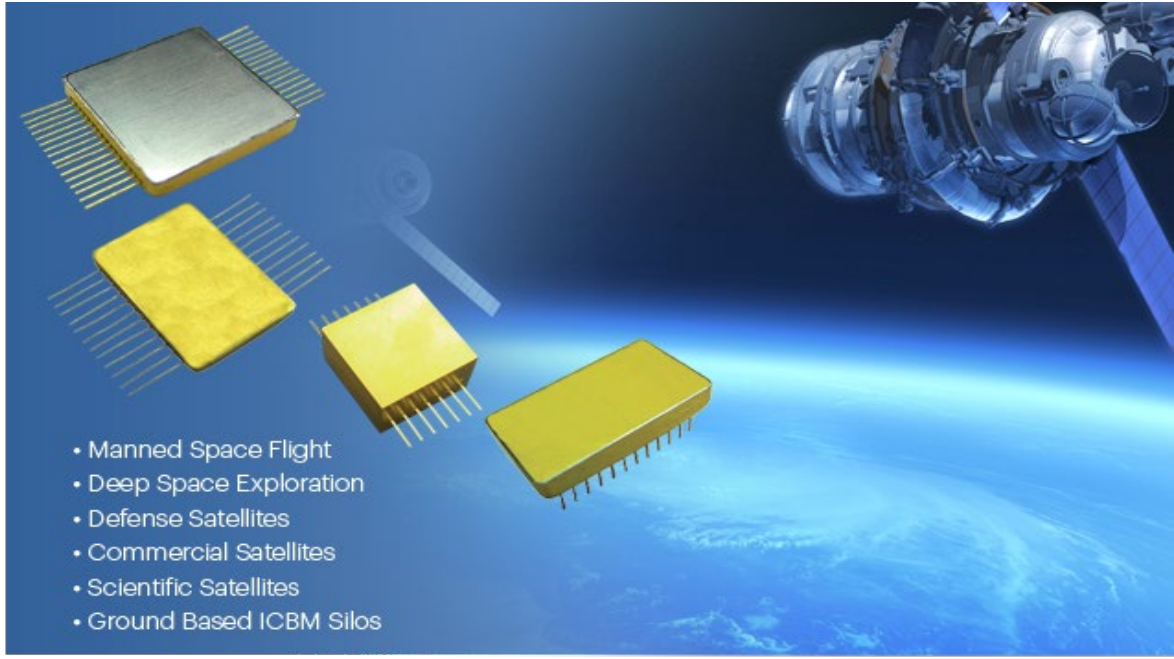
Footprint & Mass Comparison

	2101/2111 24 Pin DDIP	2102/2112 32 Lead Flatpack	2103/2113 24 Lead Flatpack	2104/2114 14 Lead Flatpack	2105/2115 14 Lead Flatpack
Dimensions (mm)	20x35x11	25x25x5	25x36x8	20x20x13	19x19x6.6
Volume (cm^3)	8	3	7	5	2.4
Footprint (cm^2)	7	6	9	4	3.6
Height (mm)	11	5	8	13	6.6
Mass (grams)	21	10	16	19	8

DOC207139, Rev B
(Released April 2019)

LVDS Hi-Rel TCXOs

- Available in single and dual complementary output pairs up to 200 MHz
- Utilizes 5962F SMD microcircuit rated to 300 krad (Si) TID
- Guaranteed no SEL to 120 MeV-cm2/mg
- Platform numbers include:
  - Single LVDS Pair (2123/2223)
  - Dual LVDS Pair (2133/2233)
- Includes typical jitter performance and phase noise plots
- Industry standard 24-pin flatpack enclosure
- Optional lead-forming available
- Recommended solder pad layout included
- Utilizes same design pedigrees, screening options and temperature stability codes as DOC200103
- Industry standard frequencies include 100, 125, 156.25 and 200 MHz



OX-249 Space Qualified OCXO
(Datasheet Revised August 2019)

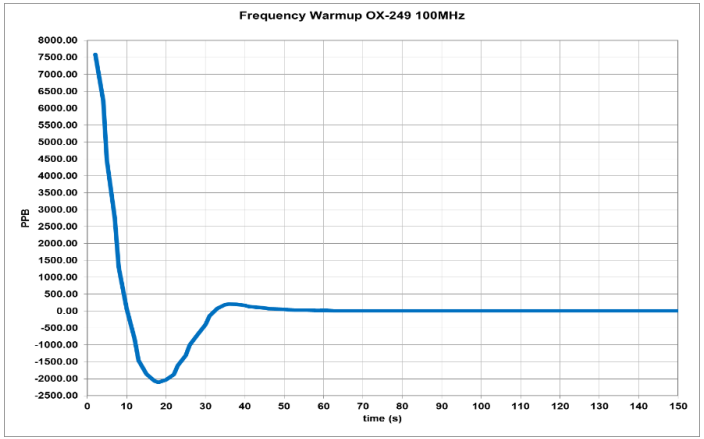
OX-249 Hi-Rel Hybrid Space Qualified OCXO

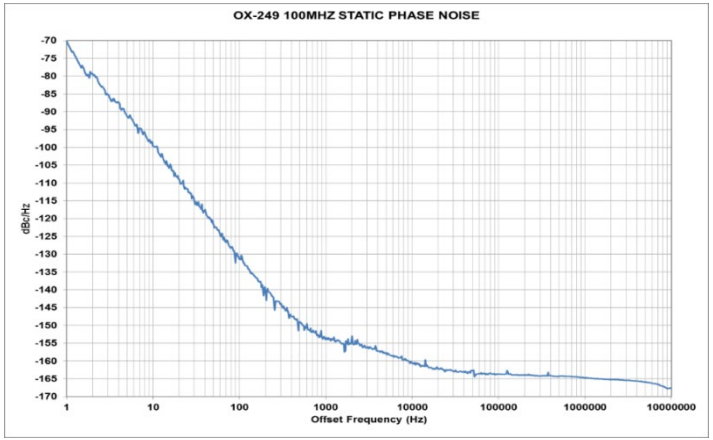
- SINE (40 to 100 MHz)
- ACMOS (10 to 100 MHz)
- LVDS (40 to 100 MHz) ** Now Available **
- Tolerant to 300 krad (Si) TID and SEL Immune
- SC-cut hermetically sealed crystal utilizes swept quartz and robust 4-point mount
- Class 2 hybrid “chip & wire” construction
- MIL-PRF-38534, Class K element evaluation
- MIL-PRF-55310, Class S quality assurance
- Meets EEE-INST-002, Level 1 derating guidelines
- Popular 24-pin DDIP enclosure
- Recently revised datasheet incorporates LVDS output option and MIL-PRF-55310, Rev F quality assurance

OX-249 Technical Advantages

- ❑ Class 2 hybrid technology provides spaceflight proven ruggedness and reliability
- ❑ Utilizes our Class S QPL manufacturing line and OCXO core competencies
- ❑ Radiation tolerant to **300 krad (Si)** TID (RLAT report available upon request)
- ❑ Achieves better than ±100ppb temperature stability
- ❑ Wide operating temperature range **(-40°C to +85°C)**
- ❑ Outstanding Allan deviation (ADEV) performance **($8x10^{-12}$ typical)**
- ❑ Optional output waveforms and wide frequency range
  - Sinewave (40 to 100 MHz)
  - ACMOS (10 to 100 MHz)
  - **LVDS (40 to 100 MHz) now available**
- ❑ No frequency multiplication
  - Exceptional phase noise floor **(-163 dBc/Hz typical)**
  - No subharmonics
- ❑ Low thermal mass (no oven block) promotes faster warm-up **(< 1 min)**
- ❑ Optional EFC w/ regulated reference voltage for frequency set or PLL facilitation

OX-249 Performance Metrics

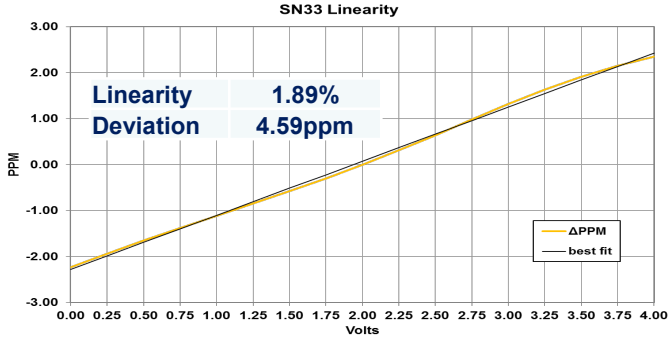




Allan Deviation $\sigma_y(\tau)$

Avg. Time (s)	Allan Deviation $\sigma_y(\tau)$	Noise Floor
1	6.27×10^{-12}	1.37843×10^{-13}
2	7.64×10^{-12}	1.12463×10^{-13}
4	7.57×10^{-12}	7.17350×10^{-14}
10	8.3×10^{-12}	2.15990×10^{-14}
20	1.03×10^{-11}	1.22945×10^{-14}
40	1.32×10^{-11}	5.67396×10^{-15}
100	1.80×10^{-11}	
200	3.1×10^{-11}	
400	5.6×10^{-11}	

$\tau_0 = 1$ s NEQ BW = 0.5 Hz



Footprint & Mass Comparison

	EX-219 EMXO Class 2 Hybrid	OX-249 OCXO Class 2 Hybrid	TX-249 TCXO Class 2 Hybrid	9800B OCXO Class 3 Mixed
Dimensions (mm)	24x26x9	20x35x10	20x35x11	34x34x34
Volume (cm^3)	5	7	8	40
Footprint (cm^2)	6	7	7	12
Height (mm)	9	9.5	11	33
Mass (grams)	7	13	21	100

- Class 2 hybrid platforms use hermetic, through-hole, Kovar/Nickel enclosures
- Class 3 mixed platforms typically use a vented, cold rolled steel or milled aluminum enclosure either with mounting screws or a mounting plate

Your Supplier of Choice

Why Vectron for Hi-Rel?

- Seven decades of spaceflight heritage
  - ✓ Proven quality track record since launch of Jupiter-C rocket in 1958
- Significant revenue re-investment in space platform R&D
  - ✓ Nearly 250 years of combined hi-rel design experience
- Broadest portfolio of space FCP content in the industry
  - ✓ Offering “all-in-one” solution for programs with multiple requirements
- Design and manufacture of space qualified platforms in the United States
  - ✓ Mount Holly Springs facility, in operation since the 1950s, is Space Center of Excellence
- Large internal capability for design, manufacturing and test
- ITAR-free space qualified platforms
- One of only two MIL-PRF-55310 Class S QPL suppliers in the world

Thank You!!!

Any Questions?