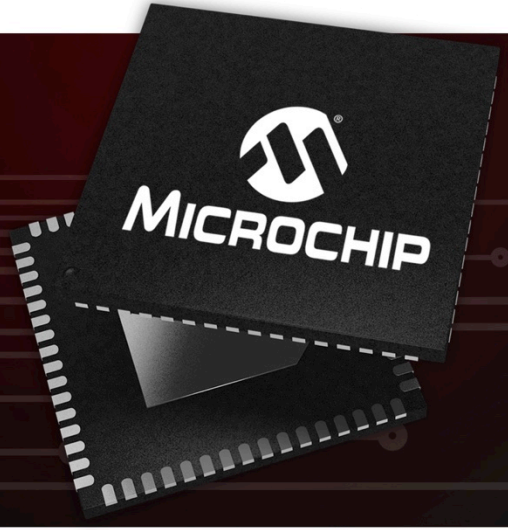
MICROCHIP



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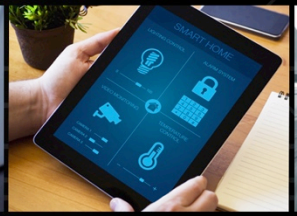



Power Module Solutions and the Basics of Rad Hardness

By: Paul L. Schimel PE

Space Forum 2019

Space Forum Outline

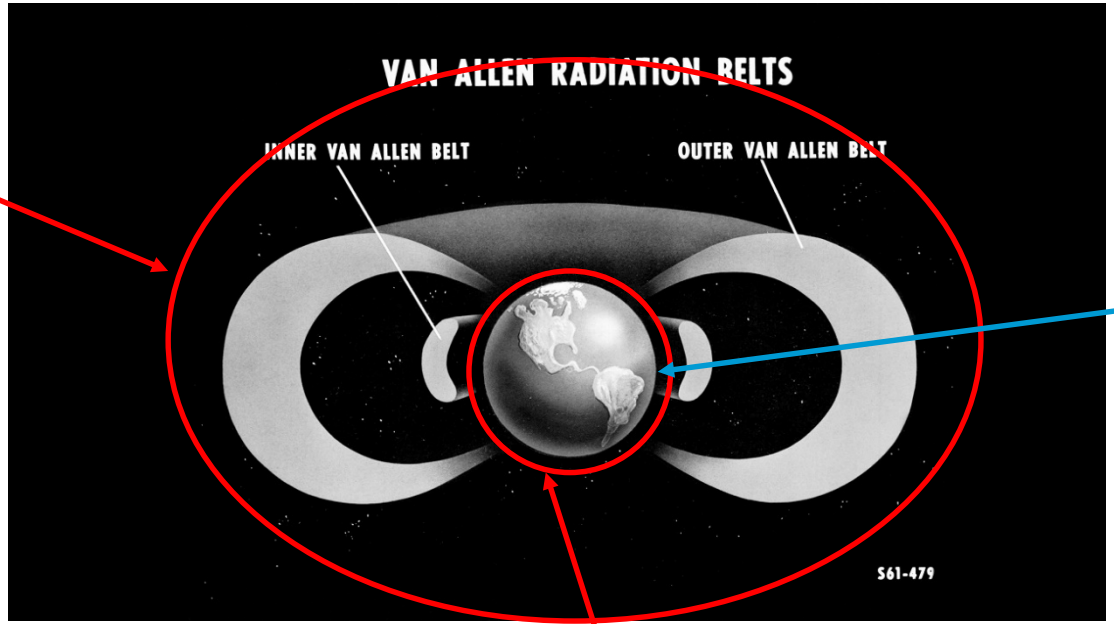
1. Why Rad Hard?
2. Bragg Distance Discussion
3. SEE Discussion
4. SEE in SiC
5. Rad Hard MOSFET Lineup
6. SiC Module Lineup (Aviation and MIL Vehicles)
7. TID Discussion
8. ELDRS Concepts
9. Neutron Bombardment Discussion
10. BJT Lineup
11. Rad Hard Power Modules
12. What Solutions Do You Need Beyond?

Why Radiation Hardened?

- The Earth's atmosphere, combined with the inner and outer Van Allen belts act as great shields to earthbound electronic equipment.
- Satellites don't get the full benefit of this shielding. The further out the satellite, the less shielding there is.
- The heavy charged particles from radiation will penetrate most metallic shielding deployed to shield and house the electronics.
- These particles can cause erratic operation and complete failure.
- A Low Earth Orbit cubesat constellation will be inside the first Van Allen belt, just above the earth's outer atmosphere.
- Some "less mission critical" LEO applications will call for simply automotive qual'd parts and NOT rad hard.
- LEO applications require less radiation hardness than higher orbits, the two Van Allen belts act as shields.
- A geosynchronous satellite orbit will fall outside of the outer Van Allen belt.
- This application will accumulate more radiation events at higher energy levels.

Why Radiation Hardened?

Geosynchronous Orbit (GEO)
- Outside both belts
- Very little shielding to impinging cosmic particle



Cosmic Particle Path
- Very little energy loss when striking target outside the belts
- Much higher energy loss/attenuation when striking target within the belts

Low Earth Orbit (LEO)
- Inside both belts
- Trapped charges and particles in the belts offer a lot of shielding to impinging cosmic particle

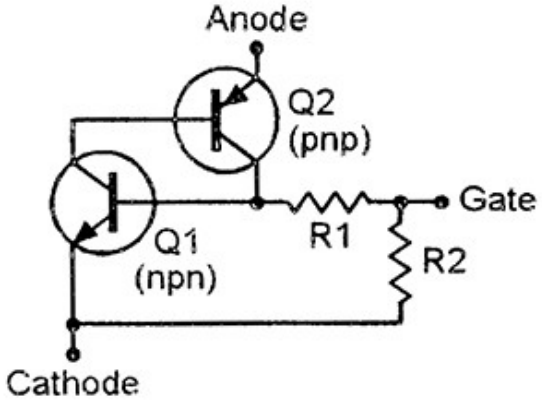
What are Effects of Radiation on Semiconductors?

- There are four main types of radiation events in semiconductors:
  - SEE (Single Event Effects)
  - TID (Total Incremental Dose)
  - ELDRS (Enhanced Low Dose Rate Sensitivity)
  - Neutron Bombardment
- There are two types of degradations:
  - Ionic
  - Lattice Disturbance
- SEE is a fast, singular event
- TID is a long-term exposure where many radiation events are captured in the device
- ELDRS is a subset of TID, carried out at a much lower dose rate
- Neutron Bombardment is an isolated test where only neutrons are passed through the DUT

A Few Words on Stopping Distance, Bragg Depth

Stopping distance (e.g.: Bragg distance, Bragg depth)

- Bragg depth is the stopping distance of the test particles. It ranges from 10um to 2000um or so (typical power device die is about 200 to 400um thick).
- Most any silicon technology has sensitive regions in this Bragg distance (drift, depletion, recombination regions and channels).
- Consider a 24-layer mixed signal IC process. PNPNPNP….SEE can cause latch-up (SEL), burn out (SEB), gate rupture (SEGR), interrupt (SEI), transient (SET) and many other anomalies.
- Different ion species have different Bragg distances.
- Bragg distance varies inversely with particle energy level. Higher energy particles have more collisions, they cause more radiation and scattering and thereby they don't penetrate as far.
- There are two mechanisms that affect Bragg distance (stopping power): collision stopping power and radiative stopping power.
- Stopping distance is determined by stopping power and density. Higher density materials will have shorter stopping distance for a given total stopping power.



Only one SCR is needed for latch-up; one PNPN stack!

Single Event Effects: SEE Test

- SEE tests are carried out in a linear accelerator
- The source delivers heavy ions or protons to the test board
- Common term is LET (Linear Energy Transfer)
- DUTS are arranged on a test board and biased accordingly (Vds max, Vgs at –Vmax (off) for MOSFETs)
- DUTS are then examined shortly after the test event
- Usually DC static measurements, leakage, gain, Vf, Rdson, etc.

TAMU Cyclotron

SEE Levels

- Common ion species, LET and energy levels

Energy Level	Ion	Total Energy	Energy at Bragg Peak	Range in Si	Range at Bragg Peak	Range To Bragg Peak	Initial LET (air)	LET at Bragg Peak
A (MeV)		MeV	MeV	um	um	um	MeV/cm^2/mg	
15	^{4}He	60	0.4	1423	2	1421	0.11	1.5
15	^{14}N	210	7	428	7	421	1.3	6.7
15	^{20}Ne	300	14	316	8	308	2.6	9.6
15	^{40}Ar	599	29	229	9	220	8	20.1
15	^{63}Cu	944	90	172	16	156	18.7	34
15	^{84}Kr	1259	152	170	21	149	26.6	41.4
15	^{109}Ag	1634	248	156	26	130	40.3	54.8
15	^{129}Xe	1934	339	156	31	124	49.3	63.4
15	^{141}Pr	2114	441	154	37	117	56	69.6
15	^{165}Ho	2474	608	156	44	112	66.7	79.2
15	^{181}Ta	2714	702	155	46	109	74.8	86.4
15	^{197}Au	2954	902	155	53	102	82.8	93.5
25	^{4}He	99	0.4	3449	2	3447	0.07	1.5
25	^{14}N	347	7	1009	7	1002	0.9	6.7
25	^{22}Ne	545	14	799	8	791	1.8	9.7
25	^{40}Ar	991	29	493	9	484	5.5	20.1
25	^{84}Kr	2081	152	332	21	311	19.8	41.4
25	^{129}Xe	3197	335	286	31	255	38.9	63.4
40	^{14}N	560	7	2334	7	2327	0.6	6.7
40	^{20}Ne	800	14	1655	8	1647	1.2	9.7
40	^{40}Ar	1598	29	1079	9	1070	3.8	20.1
40	^{78}Kr	3117	140	622	20	602	14.4	41.4
40	Proton	40	0.1	8148	1.2	8147	0.012	0.56

SEE Effects in MOSFETs and BJT

MOSFETs

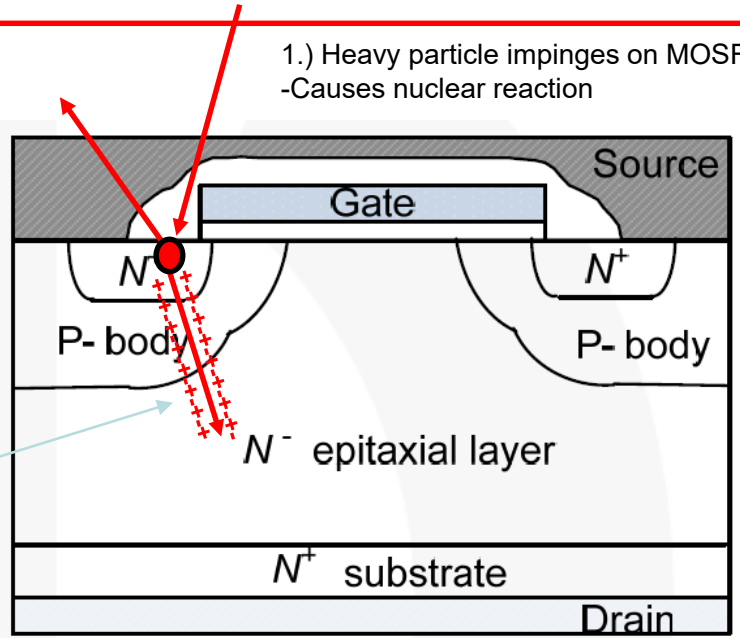
- Both SEB (Single Event Burnout) and SEGR (Single Event Gate Rupture) occur when the MOSFET is off
- SEB occurs when a heavy particle passes through the area under the source terminal
- Protons and neutrons don't normally cause SEB directly
- Indirect process involving a secondary reaction (nuclear reaction in MOSFET Si layers)
- SEB is rarer than SEGR, but still must be considered
- SEGR is the prevailing SEE in power MOSFETs

Bipolar Junction Transistor (BJT)

- SEE effects tend to be ionic, with an occasional lattice disturbance
- BJT is minimally susceptible to SEE

SEB Explanation (1)

1.) Heavy particle impinges on MOSFET surface
-Causes nuclear reaction

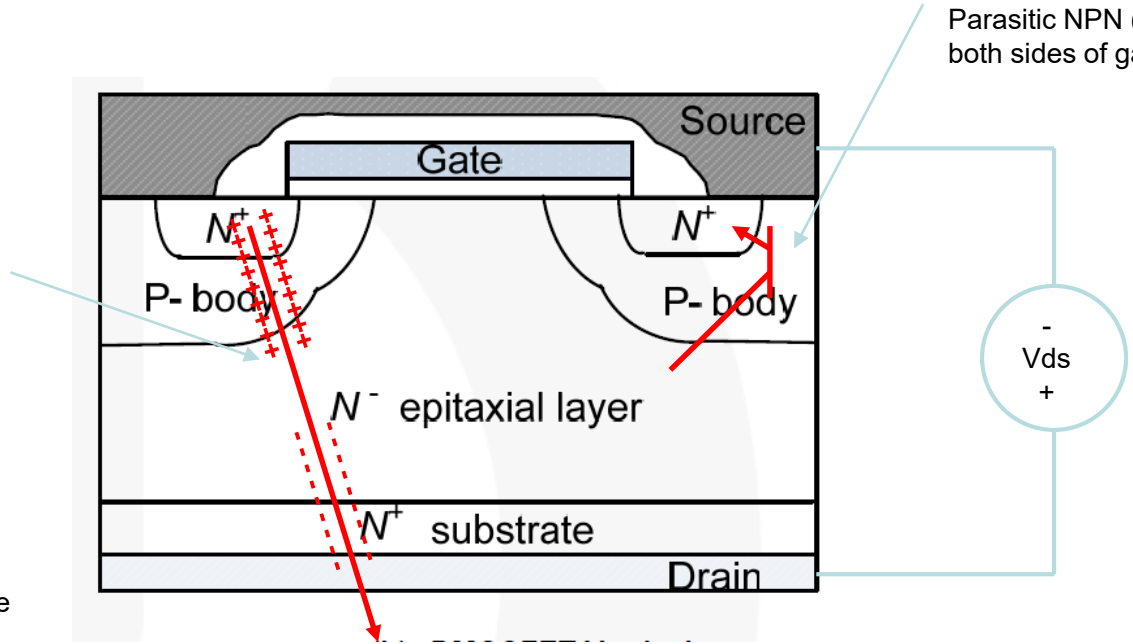


2.) Electron hole pairs created in a sheath around the reaction particle path

SEB Explanation (2)

3.) During off state (high Vds) electrons and holes migrate toward opposite charges
-Higher Vgs causes higher attraction

4.) Once enough holes accumulate in the N+, P-body region, the parasitic NPN transistor turns on
-Normally shorted by the source metallization, this transistor turns on regardless of Vgs
-causes catastrophic failure



Device off, Vgs=0V

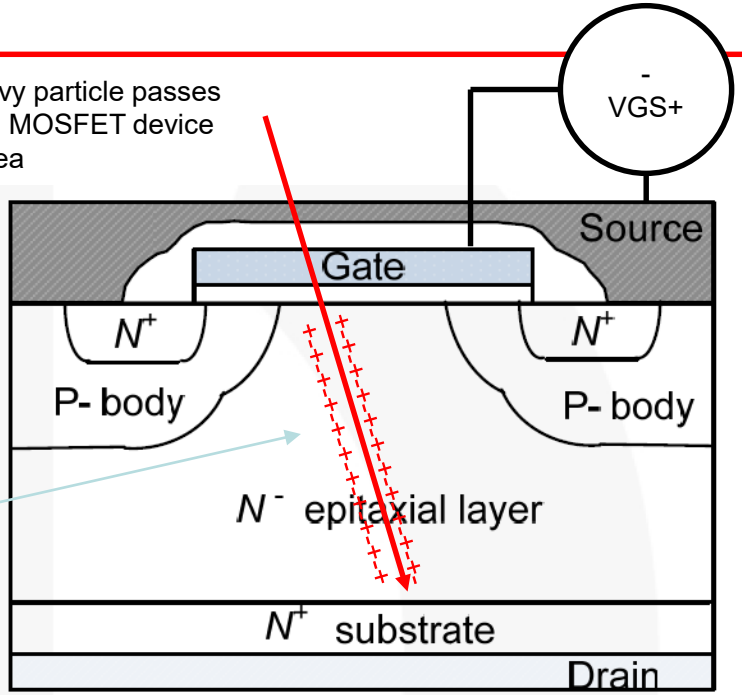
SEGR and Its Effects in MOSFETs

- SEGR occurs when a heavy particle passes through the area under the gate terminal
- Heavy charged particles cause this directly, no secondary nuclear reaction required
- SEGR conditions are –Vgs (device held well into off state), large blocking voltage (Vds is high)
- Trench MOSFETs are most susceptible to SEGR due to the very sharp trench conductor and the high electric field between this trench gate and the drain

SEGR Explanation (1)

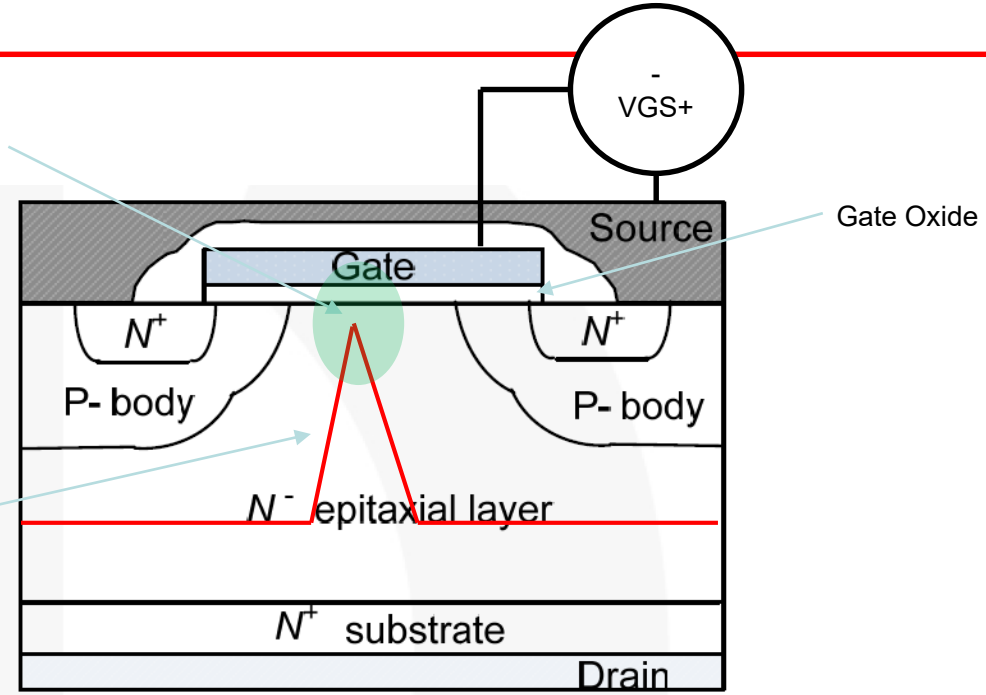
1.) Heavy particle passes through MOSFET device gate area

2.) Heavy particle creates electron hole pairs in a sheath around the particle path



SEGR Explanation (2)

Note:
- High voltage, low distance
- E-field very high
- Worst case at negative Vgs
- Can cause gate oxide to breakdown



3.) Electron hole pairs momentarily alter the channel, allowing Vd to rise up toward the P-body and the gate
- gate oxide can rupture!!!

How to Overcome SEE Effects at Circuit Design

For power switches, this is fairly straight forward.

- Derate MOSFETs. There are usually house rules for this.

Example: 120V Bus with 150V max must use at least 250V MOSFET.

- Design gate drive carefully. Turn the devices on well above Vth, turn it off such that Cdv/dt does not cause false turn on problems.

Example: Vgs on is held at 15V, Vgs off is held at -5V.

RAD Hard vs. COTS MOSFETs

- Rad hard MOSFETs are designed, tested and documented to mitigate these things as best as possible.
- With COTS parts, susceptibility could be inescapable.

SEE Effects in SiC MOSFETs

- While marvelous, SiC is not immune to SEE
- The very things that make SiC marvelous can be detrimental at SEE

SiC MOSFET

- Lower bulk resistivity in channel compared to Si MOSFET
- Higher E-field rating compared to Si MOSFET
- Combine them: used to make smaller HV power MOSFET
- SEE problems, requires intensive Vds derating
- SEGR from sharper E-field under gate at max Vds and max –Vgs
- Device redesigns are in the works
- *Very low impact from TID tests!*
- *Very low impact from Neutron Bombardment tests!*

MOSFET Lineup: Rad-Hard MOSFET (M6)

- **Device family—technical feasibility complete**
  - Vdss—100 V, 150 V, 200 V, and 250 V

- **Improved efficiency through lower switching conduction losses by lowering Rds(on) and Qgd**
  - Figure of merit (Rds(on) x Qg) improvement over competition
    - 100 V—47% (SMD0.5)
    - 150 V—90% (SMD0.5)
    - 200 V—2x (TO-254), 4x (SMD0.5)
    - 250 V—2x (SMD2), 3x (TO-254)

- **Improved Rds(on) will translate to a 10–20% higher current rating**
- **Commerce ECCN: EAR99 and 9A515.e**
- **Higher confidence level when performing worse case analysis and less de-rating**
  - SEE SOA improved over competition and functional at full-rated bias under worst case conditions (see next slide)
    - +60 MeV at full-rated BVss
  - Avalanche rating is better by design by 5x over the competition

M6 Rad Hard MOSFET Part Numbers – DLA Qual Plan

Bvdss (V)	ID1 (A)	Similar JEDEC Number	MIL-PRF-19500/SS	Industry Equivalent	Proposed Part Numbers	Package
100	22	2N7587U3	746	IRHNJ67130	JANSR2N7587U3	SMD0.5
150	19	2N7589U3	746	IRHNJ67134	JANS2N7589U3	SMD0.5
200	16	2N7591U3	746	IRHNJ67230	JANSR2N7591U3	SMD0.5
250	**12.4**	**2N7593U3**	**746**	**IRHNJ67234**	**JANSR7593U3**	**SMD0.5**

N- Ch, Sz 3

SMD0.5

Bvdss (V)	ID1 (A)	Similar JEDEC Number	MIL-PRF-19500/SS	Industry Equivalent	Proposed Part Numbers	Package
150	45	2N7582T1	753	IRHMS67164	JANSR2N7582T1	TO-254
150	56	2N7581U2	760	IRHNA67164	JANSR2N7581U1	SMD-2
200	45	2N7584T1	753	IRHMS67260	JANSR2N7584T1	TO-254
200	56	2N7583U2	760	IRHNA67260	JANSR2N7583U1	SMD-2
250	45	2N7586T1	753	IRHMS67264	JANSR2N7586T1	TO-254
250	50	2N7585U2	760	IRHNA67264	JANSR2N7585U1	SMD-2

TO-254

N- Ch, Sz 6

SMD 2

- Qualification part numbers are in yellow
- All other part numbers will be submitted to sub group E4, E6 and SEE testing (for voltage and die size only)

M6 Rad Hard MOSFET Part Numbers - Marketing

Bvdss (V)	ID1 (A)	Similar JEDEC Number	MIL-PRF-19500/SS	Industry Equivalent	Proposed Part Numbers	Package	Eng Sample Availability	Qual Date
100	22	2N7587U3	746	IRHNJ67130	JANSR2N7587U3	SMD0.5	10/15/2019	8/7/2020
150	19	2N7589U3	746	IRHNJ67134	JANS2N7589U3	SMD0.5	11/28/2019	10/16/2020
200	16	2N7591U3	746	IRHNJ67230	JANSR2N7591U3	SMD0.5	2/10/2020	11/20/2020
250	**12.4**	**2N7593U3**	**746**	**IRHNJ67234**	**JANSR7593U3**	**SMD0.5**	**7/14/2019**	**5/19/2020**

Bvdss (V)	ID1 (A)	Similar JEDEC Number	MIL-PRF-19500/SS	Industry Equivalent	Proposed Part Numbers	Package	Eng Sample Availability	Sub-Qual Only E4, E6 and SEE
150	45	2N7582T1	753	IRHMS67164	JANSR2N7582T1	TO-254	1/30/2020	3/20/2020
150	56	2N7581U2	760	IRHNA67164	JANSR2N7581U1	SMD-2	2/20/2020	4/29/2020
200	45	2N7584T1	753	IRHMS67260	JANSR2N7584T1	TO-254	3/29/2020	5/20/2020
200	56	2N7583U2	760	IRHNA67260	JANSR2N7583U1	SMD-2	4/30/2020	6/20/2020
250	45	2N7586T1	753	IRHMS67264	JANSR2N7586T1	TO-254	5/29/2020	7/30/2020
250	50	2N7585U2	760	IRHNA67264	JANSR2N7585U1	SMD-2	6/15/2020	8/30/2020

- Qualification Part Numbers are in yellow
- Other part numbers will be submitted to sub group E4 (thermal impedance characterisation), E6 (ESD characterisation) and SEE testing (for voltage and die size only)

SiC MOSFET module

Technology	Topology	BVDS (V)	Current Tc=80°C	Rdson max. per switch Tj=25°C	Package
APTMC120TAM34CT3AG	3-Phase leg	1200 V	55 A	34 mΩ	SP3F
APTMC120TAM33CTPAG			58 A	33 mΩ	SP6P
APTMC120TAM17CTPAG			110 A	17 mΩ	
APTMC120TAM12CTPAG			165 A	12 mΩ	
APTMC120HM17CT3AG	Full Bridge		110 A	17 mΩ	SP3F
APTMC120AM55CT1AG	Phase Leg		59 A	50 mΩ	SP1
APTMC120AM25CT3AG			78 A	25 mΩ	SP3F
APTMC120AM16CD3AG			98 A	20 mΩ	D3
APTMC120AM20CT1AG			108 A	17 mΩ	SP1
APTMC120AM12CT3AG			165 A	12 mΩ	SP3F
APTMC120AM08CD3AG			190 A	10 mΩ	D3
APTMC120AM09CT3AG			220 A	9 mΩ	SP3F
APTMC170AM60CT1AG		1700 V	40 A	60 mΩ	SP1
APTMC170AM30CT1AG			80 A	30 mΩ	

SP1


SP3F

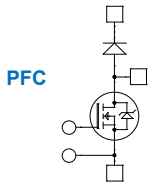

SP6P

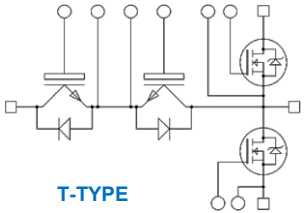

D3

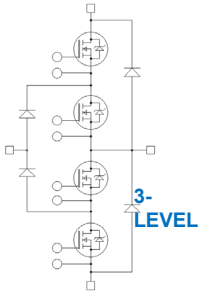
http://www.microsemi.com/product-directory/sic-modules/1347-sic-MOSFET#selection-tables

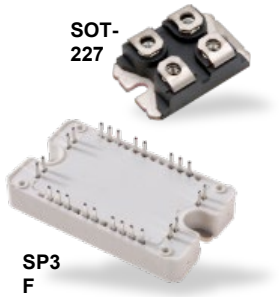
SiC MOSFET Module

PART NUMBER	TOPOLOGY	BVDS (V)	Id (A) @ Tc=80°C (A)	RdsON (mR) @ Tj=25°C	NTC	PACKAGE
APT50MC120JCU2	PFC	1200	50	40	-	SOT-227
APT100MC120JCU2			100	20	-	
APTMC120HR11CT3G	T-Type		20	110	YES	SP3F
APTMC120HRM40CT3G			50	40	YES	
APTMC60TL11CT3AG	Three Level Inverter	600	20	110	-	
APTMC60TLM55CT3AG			40	55	YES	
APTMC60TLM14CAG			160	14	-	SP6









http://www.microsemi.com/product-directory/sic-modules/1347-sic-MOSFET#selection-tables

Total Ionizing Dose: TID

- ^{60}CO Gamma ray source is used
- Tested per MIL STD883, TM1019
- Rates range from 50 to 300 rad(Si)/s
- Total ionizing dose tested from 10 Krad up to 300 Krad (and beyond in some cases)
- DUTS arranged on test board, under bias for test
- Static testing performed on DUTS after test concludes

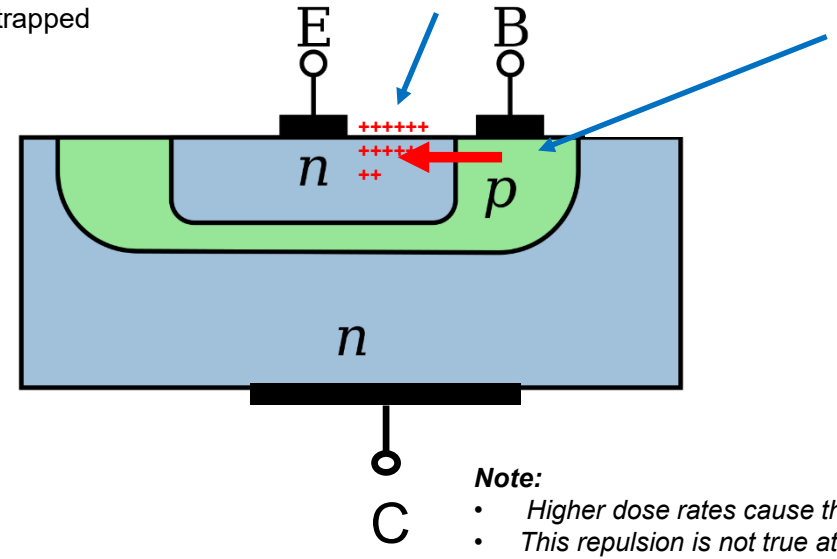
Reactor at U-Mass, Lowell

TID Effects in BJT

- BJT is susceptible to TID
- Some BJT technologies are MORE susceptible to lower dose rates—this is often heard as ELDRS (Enhanced Low Dose Rate Sensitivity)
- Heavy particle collisions create holes that accumulate on the device surface
- This accumulation steers base current away from the BE junction
- More base current must be delivered for the same collector current
- Non rad hard devices may have SEVERE degradation, whereas devices designed for this environment will have much less degradation and it will be well documented
- Net effect of TID is gain reduction in a BJT: Beta drops, HFE drops

TID Effect Explanation in BJT

- Radiation exposure creates electron hole pairs
- Trapped holes and protons accumulate on BJT surface
- More exposure = more holes and protons accumulated or trapped



- Some base current routes through this trapping
- The more holes and protons that are trapped, the more base current routes through
- This base current path contributes nothing to the collector current
- B and HFE drop off as exposure increases

Circuit Analogy:
- Trapped holes and protons shunt base current
- More trapped holes and protons, more base current shunted (R' drops)

Note:
- *Higher dose rates cause the protons and holes to repel each other*
- *This repulsion is not true at low dose rates*
- *This effect gives rise to ELDRS sensitivity*
- *The traps at low dose rates are more uniform, they can shunt more base current away*

TID Effects in MOSFET

MOSFET has two minimal effects from TID:

- Vth drops for an N channel MOSFET with increasing exposure (perhaps from 3V to 1.9V)
- Vth goes up for a P channel MOSFET with increasing TID (perhaps from 3.5V to 4.5V)
- Rdson rises slightly with increasing TID
- Idss increases slightly with increasing TID

Enhanced Low Dose Rate Sensitivity: ELDRS

- This test operates as a subset of TID
- The rates are much lower—flux in the range of 0.5mrad(Si)/s to 10mrad(Si)/s
- Total dose (fluence) of 5 Krad to 50 Krad
- This test was designed to bring out slower parametric shifts
- The primary impact is on BJTs
- Some BJTs exhibit severe gain degradation at low dose rates while performing well at normal TID levels

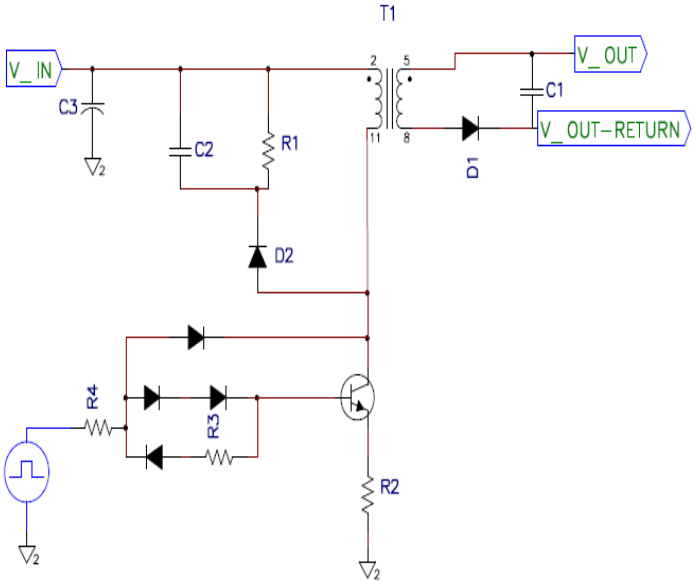
Example: How to Overcome TID and ELDRS Effects at Design Stages

Consider driving BJT with a Baker clamp circuit.

Baker clamp
- Controls Vcesat
- Steers excess drive into collector
- Controls BE storage time

At BOL the Baker clamp holds Vce sat slightly higher than traditional base drive techniques, it steers excess drive into collector

At EOL, the Baker clamp doesn't steer as much excess drive into the collector and maintains Vcesat fairly constant



Neutron Bombardment

- Straight forward test, MIL STD 883, TM1019
- DUTs are not biased, pins can be open or shorted
- Some tests simply hang a bag of parts in the beam
- Reactor applies a fast pulse, neutron detectors used to determine fluence
- DUT usually subject to neutron fluence of 5E10 n/cm^2 to 5E13 n/cm^2
- Minimal impact on MOSFETs (slight parametric shift in Rdson, Idss, Vth)
- Significant impact on BJT—Vce sat goes up, Beta/HFE drops, leakage currents go up, BE storage time DECREASES, BVceo rises (while BVcbo stays same)

Neutron Bombardment Effects

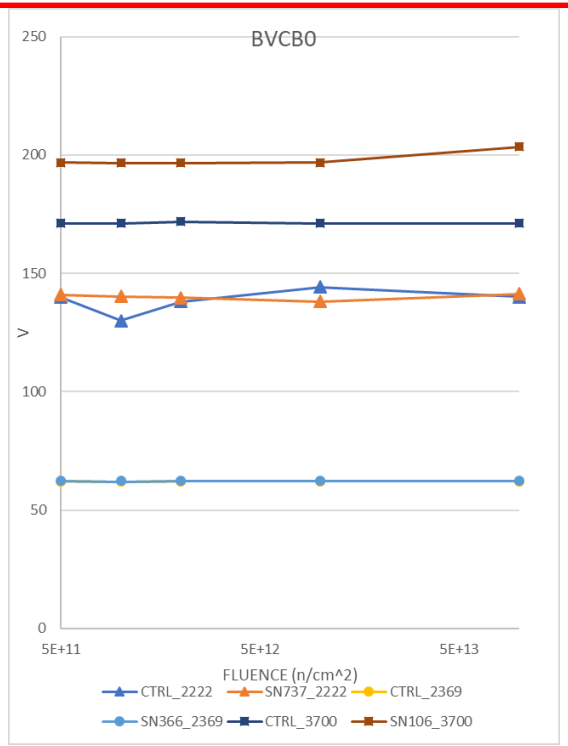


Fig. 9. BV_{CBO} vs fluence

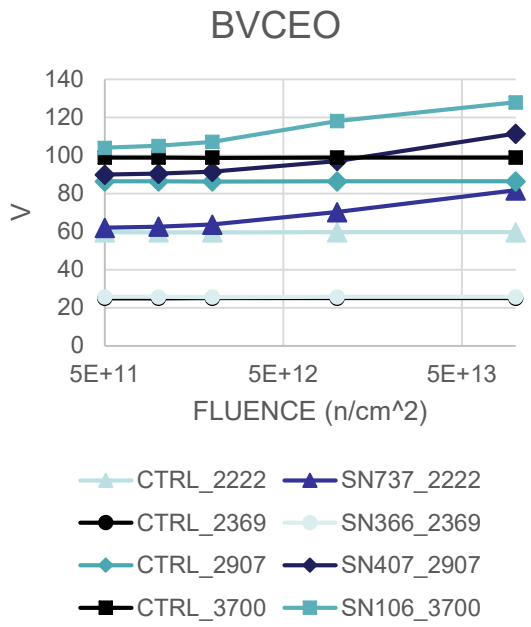


Fig. 10. BV_{CEO} vs fluence, not the slight rise compared to flat BV_{CBO}

Neutron Bombardment Effects

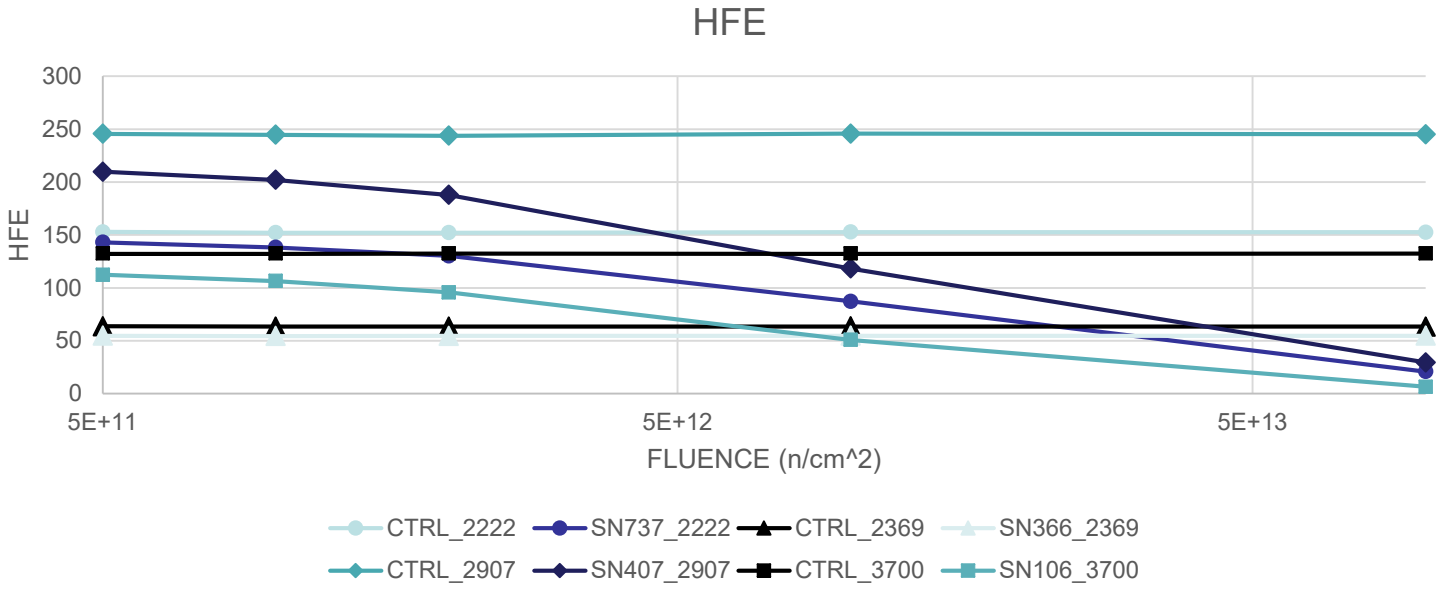


Fig. 11. h_{FE} vs fluence

In an N-Layer Mixed Signal, Mixed Mode IC Process…

- Attributes susceptible to SEE, TID, neutron and ELDRS
- Early fixes involved simply upping the bias currents on analog ICs, e.g.: UC1845 PWM controller
- Present tools still struggle with interactions, IC design for rad hard is not trivial
- Can’t “fix it in code” at mission or ATE
- Modeling software can simulate the event in top level schematic and IC layout, but the full complete impact is seldom accurate

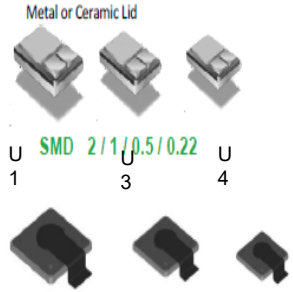
Discrete Hermetic Metal Can and Surface Mount Components

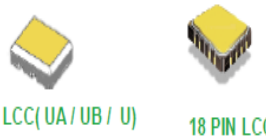
- Devices offered in metal can through-hole and SMD leadless packages
  - Bipolar Transistors (BJTs), Diodes (Schottky, Zener, TVS, Rectifiers)

Sample Set of Bipolar Junction Transistors

Part Number	Slash Sheet	Package	Polarity	Rated Voltage	Device Speed	Rated Power	Max Tj	MSC RHA Level	Qual Level	DLA Qual Level
2N2222A	/255	TO-18	NPN	50V	300ns	0.5W	200ºC	D, R, F, H	JXVSH, HKC	JXVS
2N2222AL	/255	TO-18	NPN	50V	300ns	0.5W	200ºC	D, R, F, H	JXVSH, HKC	JXVS
2N2222AUA	/255	LCC4 UA	NPN	50V	300ns	1W	200ºC	D, R, F, H	JXVSH, HKC	JXVS
2N2222AUB	/255	LCC3 UB	NPN	50V	300ns	1W	200ºC	D, R, F, H	JXVSH, HKC	JXVS
2N2222AUBC	/255	LCC3 UBC	NPN	50V	300ns	1W	200ºC	D, R, F, H	JXVSH, HKC	JXVS
2N2484	/376	TO-18	NPN	60V	60MHz	0.36W	200ºC	D, R	JXVSR	JXVS
2N2484UA	/376	LCC4 UA	NPN	60V	60MHz	0.36W	200ºC	D, R	JXVSR	JXVS
2N2484UB	/376	LCC3 UB	NPN	60V	60MHz	0.36W	200ºC	D, R	JXVSR	JXVS
2N3019	/391	TO-39KM	NPN	80V	100MHz	0.8/5W	200ºC	F	JXVSR	JXVS
2N3019S	/391	TO-39KM	NPN	80V	100MHz	0.8/5W	200ºC	F	JXVSR	JXVS
2N3501U4	/366	SMD.22 (U4)	NPN	150V	1150ns	5W	200ºC	M, R	JXV	JXV
2N3501UB	/366	LCC3 UB	NPN	150V	1150ns	0.5W	200ºC	M, R	JXVS, R, KC	JXVS
2N2907A	/291	TO-18	PNP	60V	300ns	0.5W	200ºC	R	JXVS, R	JXVS
2N2907AL	/291	TO-18	PNP	60V	300ns	0.5W	200ºC	R	JXVS, R	JXVS
2N2907AUA	/291	LCC4 UA	PNP	60V	300ns	1W	200ºC	R	JXVS, R	JXVS
2N2907AUB	/291	LCC3 UB	PNP	60V	300ns	1W	200ºC	R	JXVS, R	JXVS
2N2907AUBC	/291	LCC3 UBC	PNP	60V	300ns	1W	200ºC	R	JXVS, R	JXVS

Package	Current Rating (A)
SMD-2.0	75
SMD-1.0 (U1)	35
SMD-0.5 (U3)	15
SMD-0.22 (U4)	3
THINKEY1	100
THINKEY2	25
THINKEY3	150
THINKEY 4	75
3/4/6 PIN LCC	--
18 PIN LCC	--





Quality and Screening Flows (Military Grade)

- **MIL-PRF-19500** **[Radiation Hardness Assurance (RHA); bipolar transistors]**
  - JAN (Joint Army Navy)
  - JANTX (Extra Testing)
  - JANTXV (Extra Testing + Visual)
  - JANS (**Full Space Screening**)
    - Different radiation hardness assurance (RHA) levels (M, D, P, L, **R,** F)
  - JANHC - TX Level LAT / testing for Die Sales (Bare die)
  - JANKC - Space Level (JANS) LAT / testing for Die Sales
- **MIL-PRF-38534**
  - QML / **classes H and K facility**
    (highest level certification for military and space)

MIL-PRF-19500 - Performance requirements for discretes

⇩

MIL-STD-750 Test Methods

⇩

Slash Sheet – Specifications for individual device (ex. MIL-PRF-19500/123)

Hi-Rel Non-Hermetic Products (NHP) TVS (Transient Voltage Suppression)

Protection Devices
https://www.microsemi.com/product-directory/discretes/682-transient-voltage-suppressors#resources

L’est We Forget: SUN SPOT CYCLE

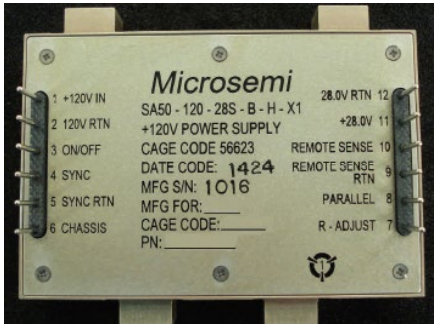
- Sunspot cycle is presently at an absolute minimum
- Sunspot activity can surge as high as 10^10 n/cm2 at sea level
- This must be understood at design

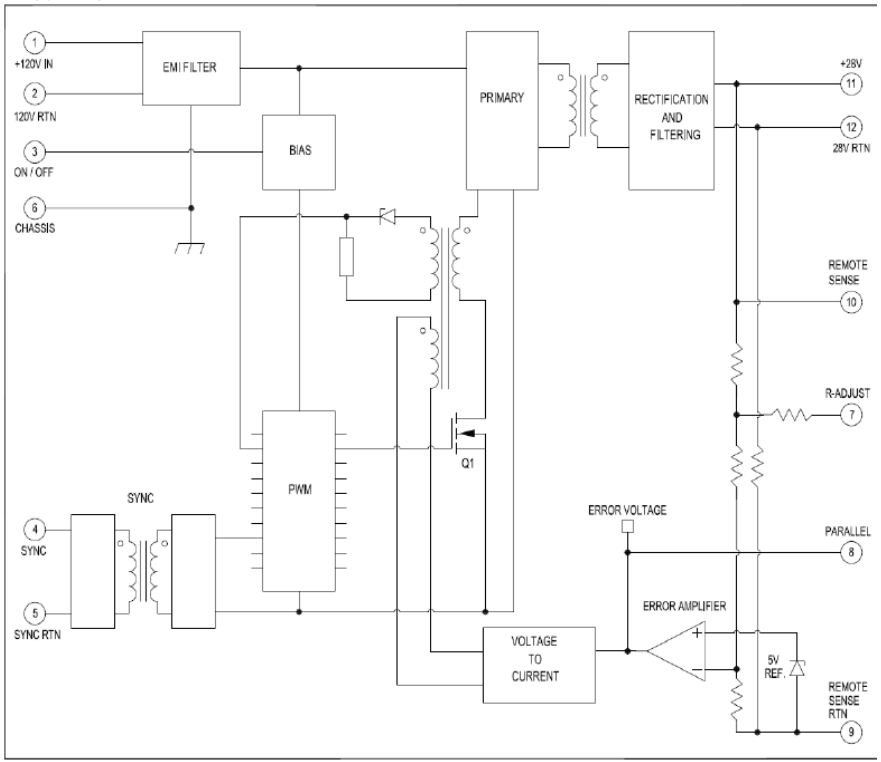
Famous Electric Car Case

[Savvy corporate counsel]:	“The accelerator stuck in 2009 because of NEUTRONS!” [counsel explains now neutrons cause soft errors in DRAM]
[practical engineer]	“OK, so then what happens when the sunspot cycle returns, perhaps with an added solar flare and the neutron fluence goes from 10^6 N/cm2 up to 10^10 N/cm2? Have you designed for that?”
[Savvy corporate counsel]:	“[nonresponse]”

SA50-120 Block Diagram

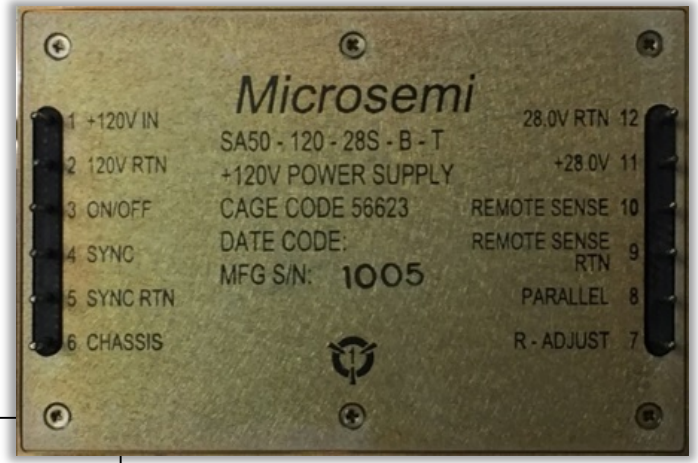
- Full Rad Hard
- Galvanically Isolated
- 86 to 150V input (120V Nominal)
- Mag Amp Regulated
- Available in Single and Dual Outputs
- 50W output; 2.05” x 3.05” x 0.475”





SA50-28 Series Space DC – DC Converters

Name :	SA50-28 Series DC – DC Converters
Description:	Satellite sub bus isolated converter
Function:	Distribute power from satellite main power bus to sub bus payload power supplies
Market:	Space power systems

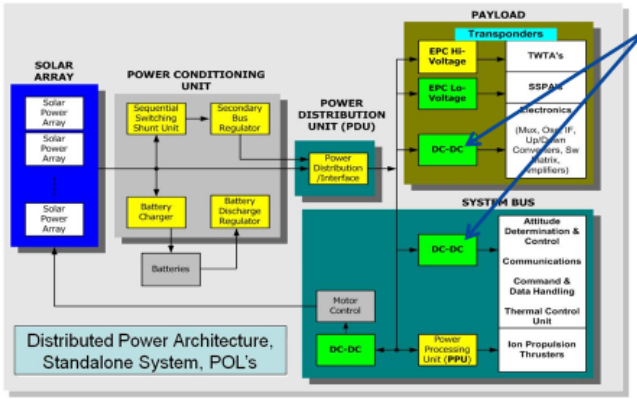


Power Level:	50W
Input:	28V Nominal; 18V – 40V Range
Outputs:	Single / Dual / Triple
Output Voltages:	28,24,15,12,5,3.3, Customized
Sync:	Isolated Sync Input
Power Enable:	All versions

Output Adjust / Remote Sense / Parallel: Single Output versions

SA50-28 Details

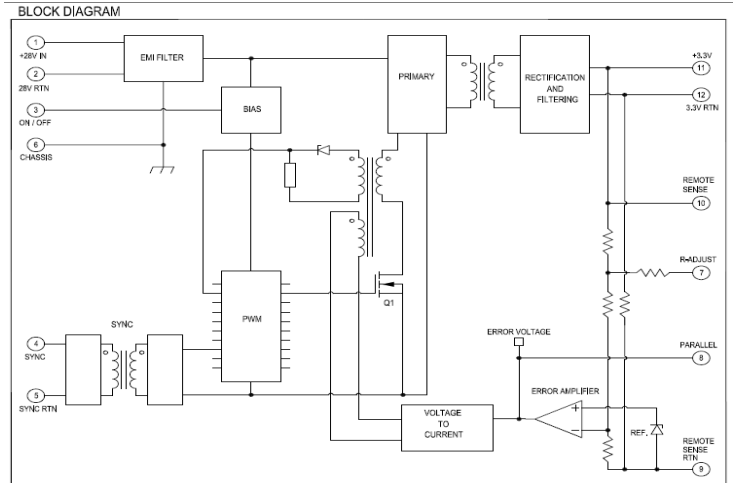
SA50 Series Applications



Applications

- Multiplexers
- IF Oscillators
- Up / Down Converters
- Matrix Amplifiers
- Altitude / general Computers
- Communications
- Command
- Thermal Control

Converts Satellite Main Bus to Local Power Bus driving Analog and Digital Electronics loads



Power Modules:
MHP50601A 3 – 7 Vin, 6 A, Synchronous Hybrid Point-of-Load DC-DC Converter

Device Features

- VIN = 3 V to 7 V (7.5V in Absolute Max)
- Internal reference (0.8 V)
- Adjustable frequency 300 kHz to 500kHz
- Parallel operation 180° out of Φ with sync pin
- Internal VREF 1.5% variation over temp and radiation
- Ultra-fast transient response to lower output impedance
- Integrated design (Cin, Cout, and Lswitch)
- Internal or optional external compensation and soft-start
- External enable or Under-voltage Lockout
- Output power good
- 96% peak efficiency

Benefits

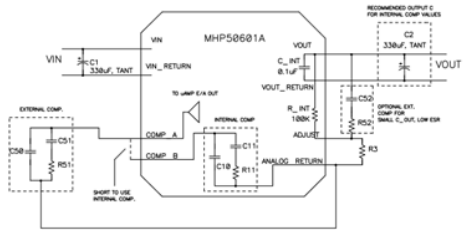
- MIL-PRF-38534 Class H or K Hybrid
- Smallest 6Amp PoL solution on the market using TPS50601A-SP Die from Texas Instruments
- Minimizes solution size through hybrid integration allowing an overall smaller point of load solution
- Optimal EMI performance though integrated hybrid design
- Radiation hardness assurance (RHA) DLA-approved TID testing follows MIL-STD-883, Method 1019.6
- Ease of implementing power sequencing schemes
- Pspice models available

Radiation Performance

- TID = 100 krad(Si), radiation hardness assured
- SEL/SEB/SEGR immune to LET 75 MeV at 125 °C
- SEFI/SET onset > LET = 65 MeV

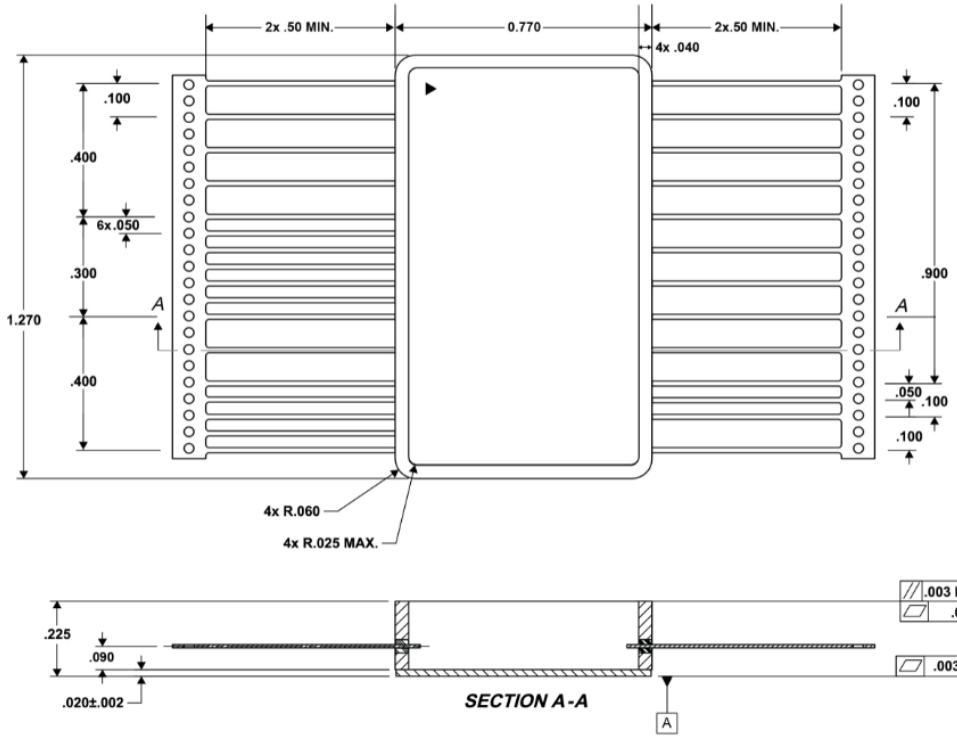
Availability:
ES Q220
Production Q320

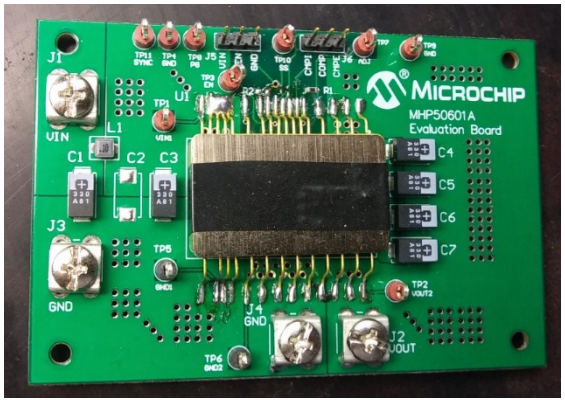
Application Circuit



MHP50601A

3 – 7 Vin, 6 A, Synchronous Hybrid Point-of-Load DC-DC Converter





Beyond!

- What solutions do you need?
- A rad hard smart switch module?
- Rad hard current sense?

Author:
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Paul Schimel is a principal power electronics engineer for aerospace and defense at Microchip Technology. He has over 23 years of theoretical and hands-on experience in power electronics spanning MIL/Aero, automotive and industrial markets. His work regularly includes module design, DC to DC converter design, device level analysis, root cause analysis, failure analysis, EMI mitigation, PCB layout, control loop compensation, inverter design, transformer design, rotating machine design, bench level measurement and validation techniques and system level analysis/comprehension. He has designed DC to DC converters from mW to MVA, inverters to 5000HP. He is a licensed Professional Engineer (PE) and holds two FCC licenses (First Class Radiotelephone and extra class amateur). Schimel holds three patents on power electronics matters. “When I get stuck, I call Paul, he figures it out,” (Prime client in A/D).

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