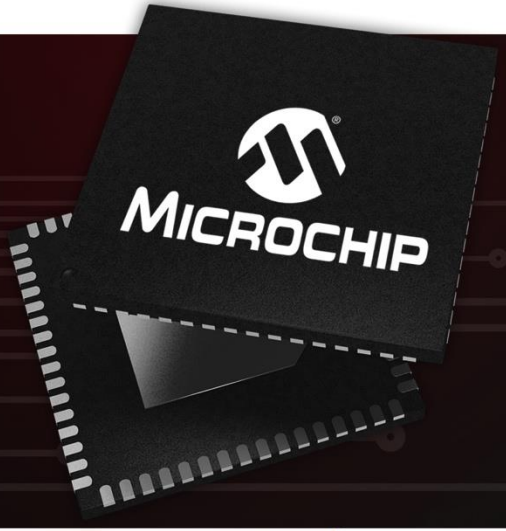
MICROCHIP



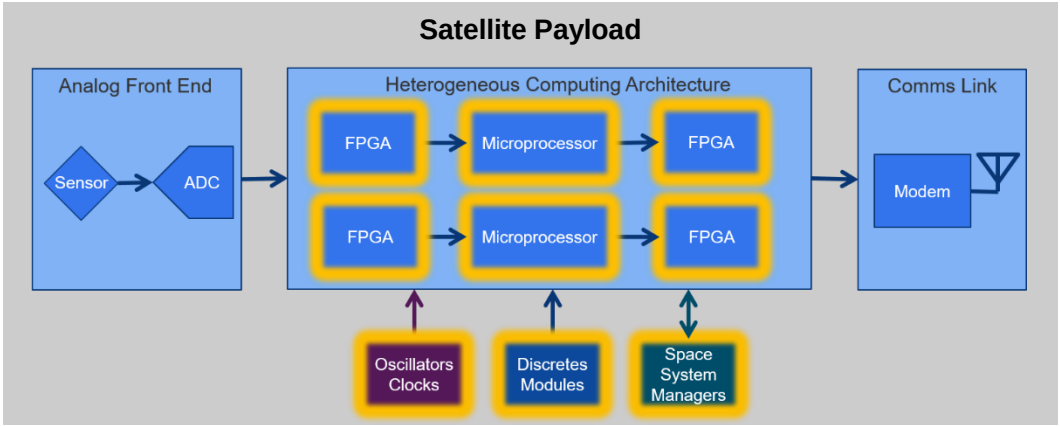
A Leading Provider of Microcontroller, Security, Mixed-Signal, Analog & Flash-IP Solutions




RT PolarFire® FPGAs
Ken O'Neill
Space Forum 2019

Achieve More Computing Throughput in Space

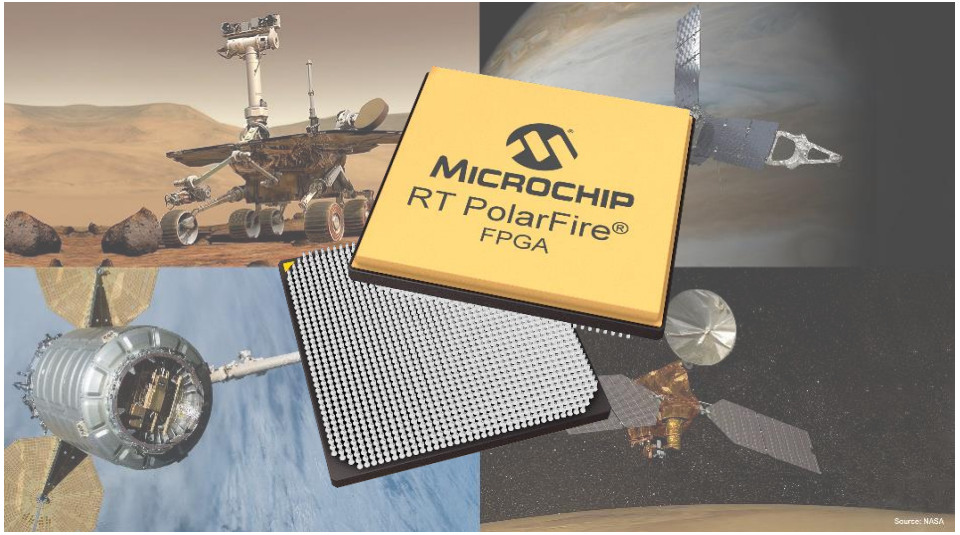
- Satellite operators demanding more information from space assets
- Sensor resolution increasing faster than available downlink bandwidth
- Faster frame rates, more channels in multi-spectral imaging
- Needs bigger, faster FPGAs with more DSP, more memory and higher I/O bandwidth
- Allows transmission of processed information, instead of raw data
- Enables autonomous decision-making on orbit



RT PolarFire®
Next-Generation Space-Qualified FPGA

RT PolarFire
- Absence of configuration upsets
- Lowest power consumption in class
- Path to QML qualification

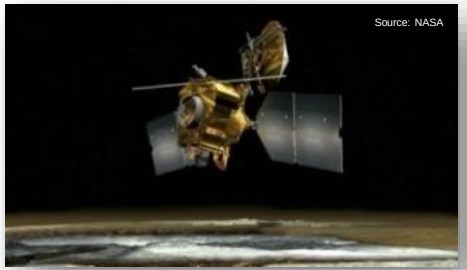
Microchip advantages
- 60+ years of space-flight heritage
- Expertise in radiation, quality, reliability
- Long-standing commitment to space



Microchip FPGA Space Flight Heritage

- **Microchip FPGAs in Space**
  - First FPGAs screened for space in 1992 (A1020 with “Extended Flow” screening)
  - First FPGAs with radiation hardening by process in 1996 (RH1280)
  - First FPGAs with radiation hardening by design in 2001 (RTSX-S)
  - First Flash FPGAs with radiation hardening by design in 2015 (RTG4)

RTSX-SU, Introduced 2004
Mars Reconnaissance Orbiter
RTSX-SU On Board (2005)



RTAX, Introduced 2005
Curiosity (Mars Science Lab)
RTAX On Board (2011)

RT ProASIC3, Introduced 2008
NASA IRIS
RT ProASIC3 On Board (2013)

RTG4, Introduced 2015
Mission Extension Vehicle 1
RTG4 On Board (2019)

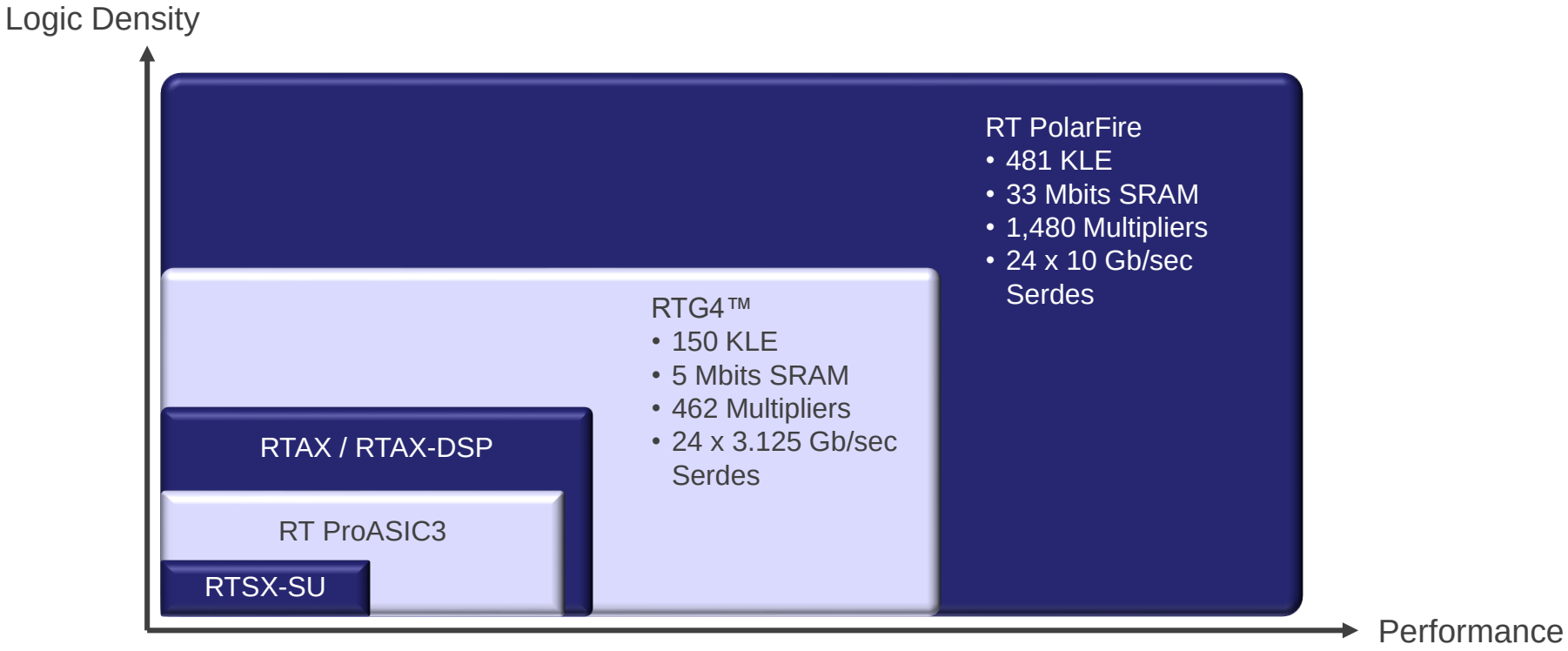
RT PolarFire® Plan

- **Commercial 28nm SONOS non-volatile and reprogrammable PolarFire die**
  - Metal layer change facilitates ceramic package integration (wider C4 bump spacing)
  - Radiation behavior characterized and reported, first report *available today*
  - Synthesized TMR, deploy where needed, *available today* in Libero SoC 12.0 and later
  - Commercial PolarFire devices and development kits *available today* for prototyping

- **Hermetically sealed, ceramic column grid array package**
  - 1509 solder columns (Six Sigma copper spiral columns)
  - Planning for QML qualification to class Q and ultimately class V

- **In development today**
  - Silicon roll out begins with engineering models in 2020, culminating in QML class V in 2023

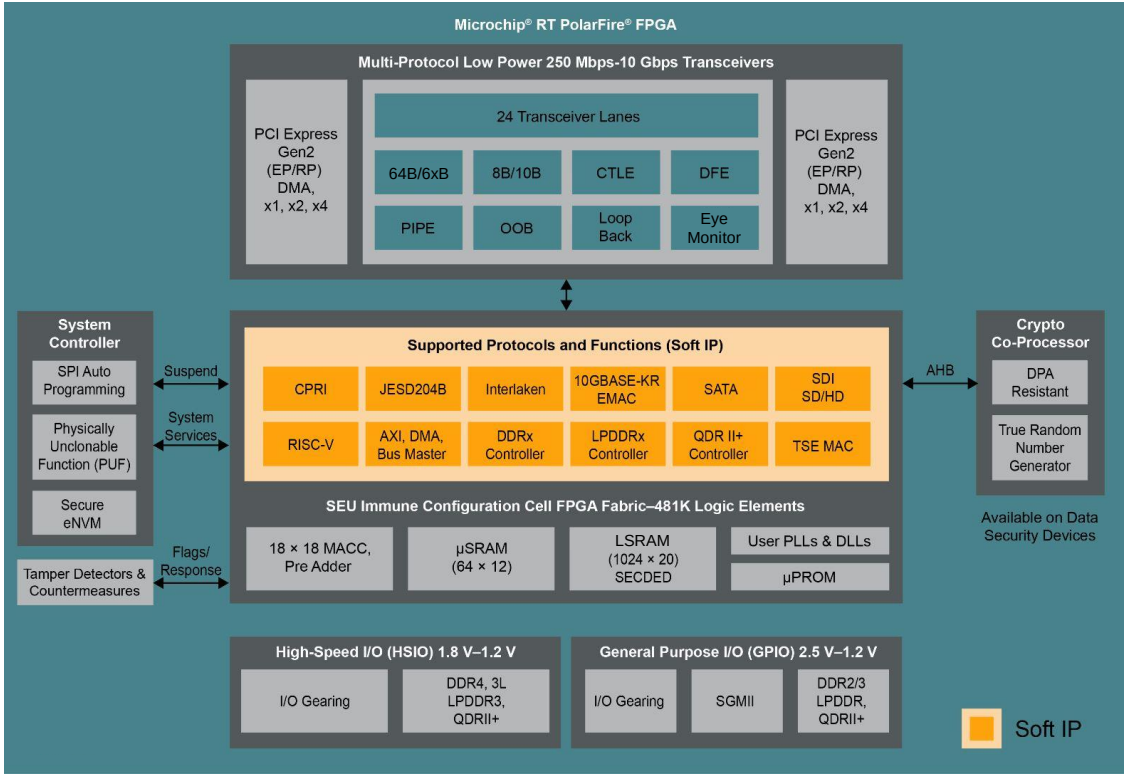
RT FPGA Families



RT PolarFire Details

Microchip RT PolarFire FPGA	RTPF500T
DFF (TMR)	0 (Instantiate Synthesized TMR Where Needed)
DFF (Non-TMR)	481K
4LUT	481K
Mathblocks (18x18 MACC)	1480
Total RAM Mbits	33 Mbits
uPROM Kbits	513 Kbits
250 Mbps - ~ 10.0 Gbps SERDES Lanes	24
I/O (HSIO/GPIO)	584 (324/260)
On Orbit Reprogrammability	To Be Characterized, TBD cycles
Radiation - TID (krad)	> 100
Radiation - SEL LET threshold (MeV-cm2/mg)	2.5V I/O > 60, 1.8V I/O > 80
Radiation - Config SEU (events/FPGA/year; GEO solar min)	None
Package	1509 CCGA
Prototyping	MPF500T RTPF500T PROTO
Qualification	Mil Std 883B planned QML class Q planned QML class V planned

RT PolarFire FPGA Architecture



Lowest Total Power: Save up to 50%

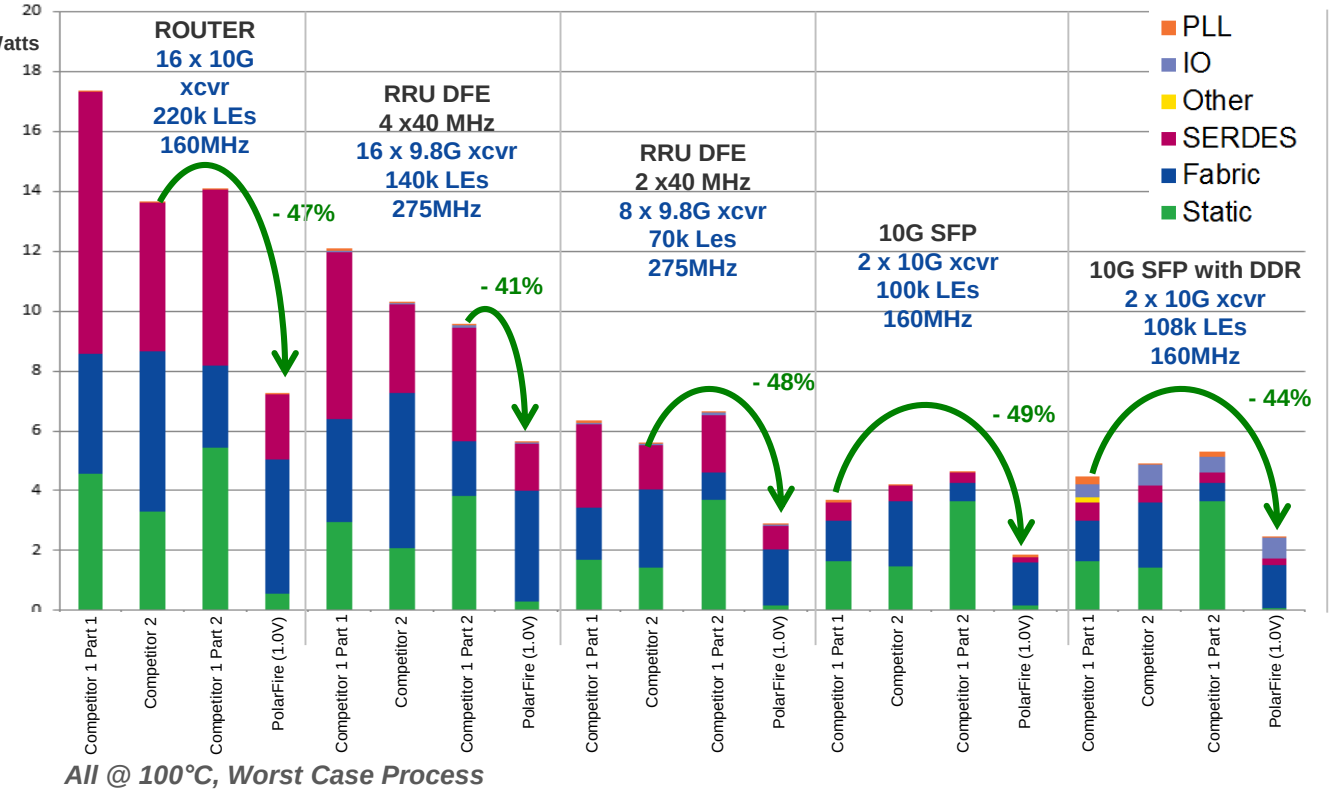
PolarFire Enables Application Performance at Significantly Lower Power

Static power
10x reduction

Transceiver power
2x reduction

Up to 50% total power savings

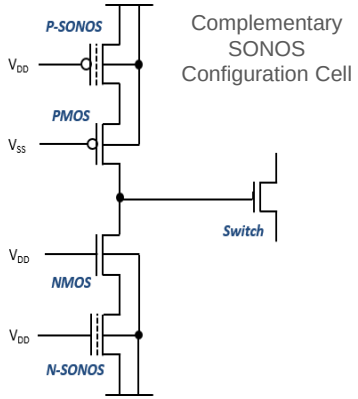
- ***Easier power supply design***
- ***Easier thermal management***



All @ 100°C, Worst Case Process

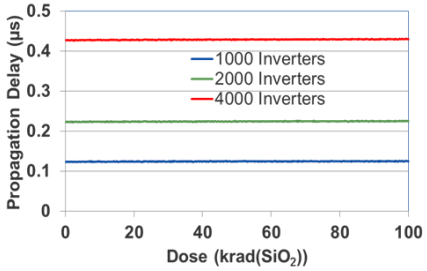
RT PolarFire Radiation (1)

- **Measuring total dose effects in RT PolarFire**
  - Retention effects in SONOS are considered
  - TM1019 testing is combined with retention tests
  - Initial experiments determined that retention test followed by TID test causes more severe degradation in SONOS than TID test followed by retention test
- **Total dose results**
  - TID effects mitigated by complementary push-pull SONOS configuration cell, similar to RTG4
  - RT PolarFire capable of 100 krad TID at constant 110°C for 10 years

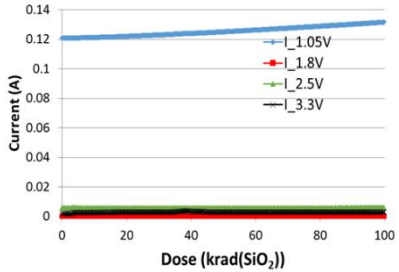


Complementary SONOS Configuration Cell

Negligible Change in Delay in Inverter Chains to 100 krad (Includes Retention Effects)



Slight Change in IDD Static Current to 100 krad (Includes Retention Effects)

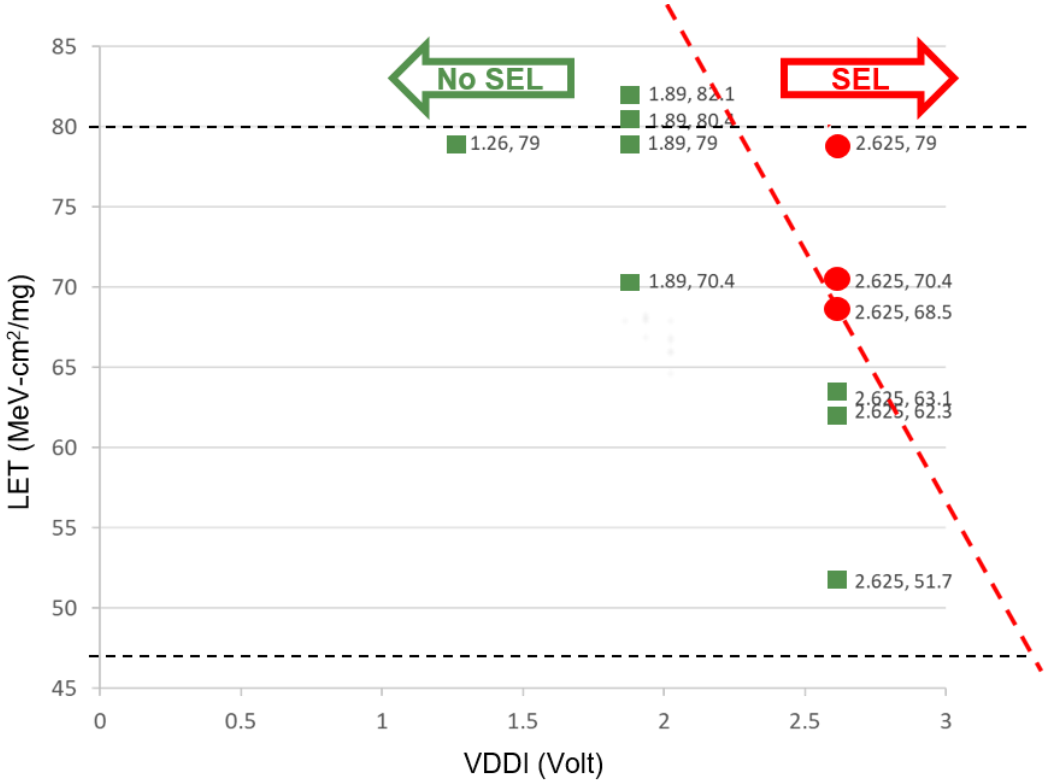


RT PolarFire Radiation (2)

- **Single Event Configuration Upsets**
  - In multiple tests, with total fluence > 5E7 ions/cm^2 up to LET > 80 MeV-cm^2/mg, no configuration upsets have been detected
- **Single Event Latch-Up**
  - SEL in I/Os
    - When running at 3.465V (3.3V +5%), 100°C, onset LET threshold between 25 and 48 MeV-cm^2/mg
    - When running at 2.625V (2.5V +5%), 100°C, onset LET threshold between 63 and 68.5 MeV-cm^2/mg
    - When running at 1.890V (1.8V +5%), 100°C, onset LET threshold higher than 80 MeV-cm^2/mg
- **Single Event Functional Interrupt**
  - SEFI causes part to enter reset state and recover
  - Orbital rate is once per 40 years, GEO solar min

RT PolarFire Radiation (3)

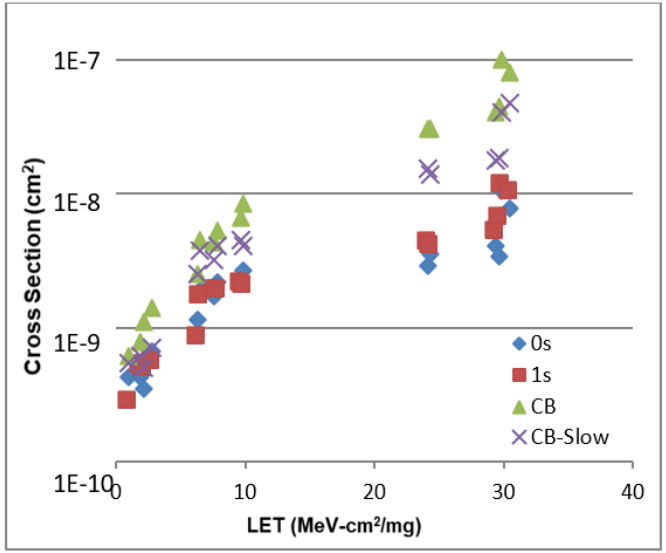
	1.26V I/O	1.575V I/O	1.89V I/O	2.625V I/O
LET 60				No SEL >1E7 ionscm^2
LET 65				SEL Detected ~9E6 ions/cm^2
LET 70			No SEL >1E7 ions/cm^2	SEL Detected ~4.4E5 ions/cm^2
LET 75	No SEL >1E7 ions/cm^2		No SEL >1E7 ions/cm^2	
LET 80			No SEL >1E7 ions/cm^2	SEL Detected <1.2E6 ions/cm^2



RT PolarFire Radiation (4)

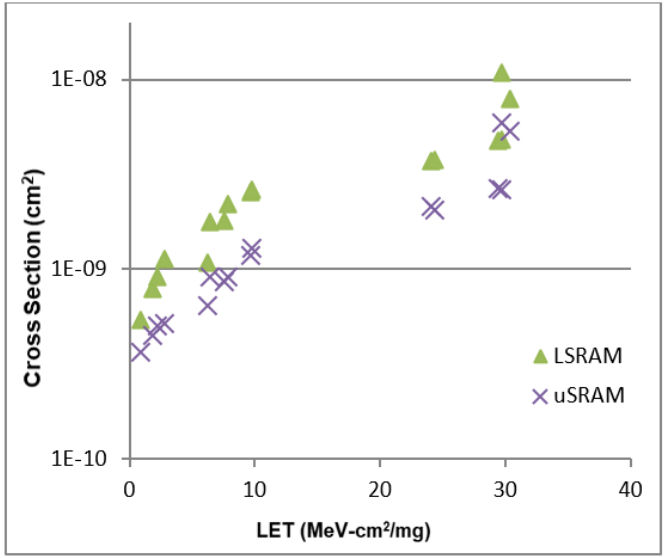
- **Single Event Upset Rates**
  - Unprotected flip-flops (no synthesized TMR)
    - All-1 and All-0 data patterns upset at ~ 4.1E-8 errors/bit-day, GEO Solar Min, 0.1” Al
    - Checkerboard data pattern upsets at ~ 2.3E-7 errors/bit-day, GEO Solar Min, 0.1” Al

Flip-flop SEU



RT PolarFire Radiation (5)

- **Single Event Upset Rates**
  - Unprotected SRAM (no EDAC, no scrubbing)
    - LSRAM blocks (20kbit) upset at ~ 4.4E-8 errors/bit-day, GEO Solar Min, 0.1” Al
    - uSRAM blocks (768bit) upset at ~ 9.2E-8 errors/bit-day, GEO Solar Min, 0.1” Al



SRAM SEU

- **Next Steps**
  - Planning to test Mathblocks, SERDES, PLL, protected flip-flops and SRAM, clock networks, SETs, reprogramming in radiation . . .

Start Designing Today

- **PolarFire commercial FPGAs**
  - Shipping in volume today, use MPF300 or MPF500 to start RTPF500 designs

Features	PolarFire FPGA			
	MPF100	MPF200	MPF300	MPF500
Logic Elements (4LUT + DFF)	109K	192K	300K	481K
Math Blocks (18x18 MACC)	336	588	924	1480
Total RAM (Mbits)	7.6 Mbits	13.3 Mbits	20.6 Mbits	33 Mbits
Available	Now	Now	Now	Now

- **PolarFire development kits**
  - Development kits available today which can be used to develop RT PolarFire designs

- **Libero development software**
  - Libero SoC 12.0 and later supports synthesized triple modular redundancy (TMR) for SEU protection in flip-flops

Summary

- **RT PolarFire next generation space-qualified FPGA**
  - Higher density and performance for high speed on-board processing
  - Significant power savings relative to other FPGAs at this density level
  - Free of configuration upsets, single chip implementation, no scrubbing
  - Path to full QML class Q and class V qualification

RT PolarFire Schedule:

- Silicon roll out begins with engineering models in 2020, culminating in QML class V in 2023

Available Today:

- Libero synthesis support for TMR
- Commercial PolarFire evaluation kit (MPF300)
- MPF300 and MPF500 FPGAs for prototyping
- Power calculator