AVR128DB28/32/48/64

AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications

The AVR128DB28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002247), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DB28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002247) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- Erratum is not applicable.

X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A4(1)	Rev. A5
Device	2.2.1 Some Reserved Fuse Bits are '1'	X	-
ADC	2.3.1 Increased Offset in Single-Ended Mode	X	-
CCL	2.4.1 The Entire CCL Module Needs to be Disabled to Change the Configuration of a Single LUT	X	X
	2.4.2 The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32-pin Devices	X	-
CLKCTRL	2.5.1 External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready	X	-
	2.5.2 RUNSTDBY is Not Functional When Using External Clock Sources	X	-
PORT	2.6.1 PD0 Input Buffer is Floating	X	X
OPAMP	2.7.1 OPAMP Consume More Power Than Expected	X	-
	2.7.2 The Input Range Select is Read-Only	X	-
RSTCTRL	2.8.1 BOD Registers Not Reset When UPDI is Enabled	X	-
TWI	2.9.1 The Output Pin Override Does Not Function as Expected	X	X
USART	2.10.1 Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X
	2.10.2 Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode when RXCIF is '0'	X	X
ZCD	2.11.1 All ZCD Output Selection Bits are Tied to the ZCD0 Bit	X	-

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits are '1'

For material with date code 2021 (year 2020, week 21) or older, the default fuse values are not compliant with the data sheet.

The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (Device will use the OSCHF clock source)
- SYSCFG0 = `0xF6`
- SYSCFG1 = `0xE8`

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.3 ADC - Analog to Digital Converter

2.3.1 Increased Offset in Single-Ended Mode

The ADC result has a typical offset of -3 mV (V_{DD} = 3.0V, Temp = 25°C) when the ADC is operating in single-ended mode.

The typical offset drift vs. V_{DD} is -0.3 mV/V, and the typical offset drift vs. temperature is -0.02 mV/°C.

Work Around

To reduce the offset, use the ADC in differential mode and connect the negative ADC input pin externally to GND.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.4 CCL - Configurable Custom Logic

2.4.1 The Entire CCL Module Needs to be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL module will first need to be disabled. Since the enable control bit will disable all the LUTs, this might cause issues if different LUTs are used for independent tasks.

Work Around
None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.4.2 The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32-pin Devices

When using INSELn to select the LINK input option for LUT3, the actual output connection from LUT0 does not get connected as an input to LUT3. This occurs only on the 28-pin and 32-pin devices.

Work Around
Do not select LINK mode for LUT3 with INSELn.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5 CLKCTRL - Clock System

2.5.1 External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready

If an external clock source is selected (SELHF in XOSCHFCTRLA is '1') and the Run Standby (RUNSTDBY) bit in XOSCHFCTRLA is '1' without the clock source being requested, the External Clock/Crystal Status (EXTS) bit will not be set to '1' when the external clock source is ready.

Work Around
Request the clock from RTC or TCD before checking the EXTS bit.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5.2 RUNSTDBY is Not Functional When Using External Clock Sources

When using any of the External Clock Sources, the related Run Standby bit (RUNSTDBY), found in the XOSC32KCTRLA register, will not force the oscillator source to stay on during sleep modes.

Work Around
Enable a peripheral, with the external oscillator as the clock source, to keep the clock source active during sleep modes.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.6 PORT - I/O Pin Configuration

2.6.1 PD0 Input Buffer is Floating

On 28-pin and 32-pin package parts, the PD0 input buffer is floating. Because the default direction setting for PD0 is as an input pin, this may cause unexpected current consumption.

Work Around

Disable the PD0 input (ISC in PORTD.PIN0CTRL) or configure the pin as an output (bit 0 in PORTD.DIR).

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.7 OPAMP - Analog Signal Conditioning

2.7.1 OPAMP Consume More Power Than Expected

The OPAMP module consumes up to three times more current than specified when the output is driven closer to either the upper or lower rails.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.7.2 The Input Range Select is Read-Only

The Input Range Select (IRSEL) bit is read-only. When the Analog Signal Conditioning (OPAMP) peripheral is active, the input voltage range will be rail-to-rail.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.8 RSTCTRL - Reset Controller

2.8.1 BOD Registers Not Reset When UPDI is Enabled

The registers VLMCTRL, INTCTRL and INTFLAGS in BOD will not be reset by other reset sources than POR if the UPDI is enabled.

Work Around
None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.9 TWI - Two-Wire Interface

2.9.1 The Output Pin Override Does Not Function as Expected

When TWI is enabled, it overrides the output pin driver, but not the output value. So when the value in the PORTx.OUT register is '1', for the pins corresponding to the SDA or SCL, the output on the line will always be high.

Work Around
Ensure that the value in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.10.1 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of Open-Drain mode being enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10.2 Start-of-Frame Detection Can Unintentionally Be Enabled in Active Mode when RXCIF is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '0'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects

the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data.

Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode, so no interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register, when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.11 ZCD - Zero-Cross Detector

2.11.1 All ZCD Output Selection Bits are Tied to the ZCD0 Bit

The output selection bits, ZCD1 and ZCD2, are tied to bit ZCD0. When writing a value to ZCD0, all three ZCD outputs are switched from the default pin setting to the alternative pin setting. When writing to either ZCD1 or ZCD2, nothing happens.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002247).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Comments
A	08/2020	Initial document release

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