

## Rad-Hard 32-bit Arm® Cortex®-M7 Microcontroller for Aerospace Applications Errata Sheet

### SAMRH71 Errata

The device that you have received conforms functionally to the current Data Sheet (Rad-Hard 32-bit Arm® Cortex®-M7 Microcontroller for Aerospace Applications), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for the silicon revision SAMRH71F20C and are summarized in the following table [Silicon Issue Summary](#).

### Silicon Issue Summary

**Table 1. Silicon Issue Summary**

Module	Feature	Errata Number	Summary
ARM® Cortex®	M7 ARM® Cortex®-M7	<a href="#">1</a>	All issues related to the r1p1 (and MRLB) core is described on the ARM site.
PIO	Cold sparing	<a href="#">2</a>	Some PIOs are not cold sparing compliant.
PIO/FlexCOM	Internal pull up value	<a href="#">3</a>	The internal pull up values are not compliant with TWI standard.
NMIC	External crystal 32 KHz frequency monitoring NMIC input	<a href="#">4</a>	External crystal 32 KHz frequency monitoring not possible
NMIC	Default VDDCORE polarity	<a href="#">5</a>	Default VDDCORE polarity not aligned with NMIC default configuration
NMIC	NOFIX_FlexRAM input	<a href="#">6</a>	NOFIX_FlexRAM input is not available as NMIC source.
HEFC/Debugger	Flash versus debugger selection	<a href="#">7</a>	Debugger link selection could be dependent on the HEFC flash activation/deactivation.
SPW	Discard option not available	<a href="#">8</a>	Space wire discard option is not available
HEMC/HECC	CFG2 and CFG3 pin value	<a href="#">9</a>	The CFG2 and CFG3 pins values are not written in the correct register
HSDRAMC/HECC	UNAL bit not compliant with HECC	<a href="#">10</a>	When HECC is activated on HEMC/HSDRAMC, the UNAL option shall be OFF
HMATRIX	Hmatrix protection	<a href="#">11</a>	Masters could not access slaves if hmatrix permissions access are not removed.
ICM/HEMC/HECC	HECC faulty address register	<a href="#">12</a>	HECC faulty address register is not correct for HEMC memories in the case of ICM (and its DMA) is running in parallel.
1553	1553 - Interrupt not triggered in case of transmission without status word	<a href="#">13</a>	1553 - Interrupt not triggered in case of transmission without status word

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## 1. CortexM7 r1p1 Errata

### **Issue**

ARM® Cortex®-M7

All issues related to the ARM r1p1 core is described in the ARM website.

### **Workaround**

Refer to the following ARM documentation:

- ARM Cortex-M7 r1p1 core (MRLB device):  
<https://silver.arm.com/download/download.tm?pv=3257391&p=1929427>
- ARM Embedded Trace Macrocell CoreSight ETM-M7 (TM975) Software Developers Errata Notice: <https://silver.arm.com/download/download.tm?pv=1998309>

## **2. Cold Sparing**

**Issue**

The following pins are not cold sparing compliant PA1, PA7, PA13, and PA17

**Workaround**

None

### **3. FlexCOM\_TWI: Internal Pull up**

**Issue**

The internal pull up value embedded in SAMRH71 is not compliant with the flexCOM TWI standard.

**Workaround**

Use external pull up of 2.2 K $\Omega$ .

#### **4. NMIC: Xtal\_32k\_fail**

**Issue**

Since the internal RC 32 KHz is not trimmed, monitoring frequency of the external 32 KHz crystal (Xtal\_32KHZ) is not possible.

**Workaround**

None

## 5. **NMIC: Bad VddCore Polarity**

### **Issue**

The internal NMIC\_VDDCORE\_Fail input signal polarity is inverted (active low) and the default configuration of the NMIC\_NMI4 (NMIC\_VDDCORE\_Fail) source is active high. As a result, the corresponding interrupt is continuously triggered.

### **Workaround**

Configure the polarity of NMIC\_NMI4 (NMIC\_VDDCORE\_Fail) source to active low in NMIC\_SCFG4R.POL bitfield.

**6. NMIC: NOFIX\_FlexRAM Source is not Connected****Issue**

NOFIX\_FlexRAM NMIC is not connected as a NMIC source input (NMI8 source).

**Workaround**

None



## 7. JTAG Debug Mode not Reachable when Flash is Disabled

### **Issue**

The flash memory of the SAMRH71 can be enabled/disabled by software.

The Debug mode selection (JTAG/SWD) is selected by GPNVM1 that is stored in the flash, thus leading to availability of the GPNVM1 only when the flash is enabled.

- When the flash is enabled, both JTAG and SWD debug modes are accessible.
- When the flash is disabled, only SWD debug mode is accessible.

By default, the SAMRH71 debug mode is configured for debug in SWD mode.

### **Workaround**

- Full debug sessions execution in SWD mode.
- Do not disable the flash while in Debug mode, then JTAG could still be used.

## 8. Space Wire (SPW): Discard Option on Receiver Does not Discard Packets as Expected

### Issue

On a receive test with data input faster than the process time required by the system to handle the packet, the expected behavior is that the receiver discards incoming packet as there is no current buffer to handle them.

When the receiver has not been active, and discard mode is activated on reset, packet received are discarded correctly. But when the receiver has been active and has already received data, even if there is no current buffer (but buffer is locked in previous mode), incoming packets are not discarded anymore.

### Workaround

The DISCARD option in the space wire link register is deactivated.

## 9. HEMC and HECC: Values of CFG2 and CFG3 are not Written in Correct Register after Reset

### Issue

When reset is released, the HEMC\_CR\_NCS0.ECCENABLE value depends on the pin value of CFG2. The value of CFG2 pin can not be read in the HEMC\_CR\_NCS0.ECC\_ENABLE bitfield, as expected but in the

HEMC\_HECC\_CR0.bitfield0 instead.

When reset is released, the HEMC\_CR\_NCS0.ECC12\_ENABLE value depends on the pin value of CFG3. The value of CFG3 pin can not be read in the HEMC\_CR\_NCS0.ECC12\_ENABLE bitfield, as expected but in the HEMC\_HECC\_CR0.bitfield3 instead.

However, when the user wants to change the values by writing in the registers, it could be done through the HEMC\_CR\_NCS0 register.

### Workaround

The value applied by CFG2 pin when the reset is released shall be read in the HEMC\_HECC\_CR0.bitfield0 first and transfer to HEMC\_CR\_NCS0.ECC\_ENABLE bitfield to avoid any issue later on.

The value applied by CFG3 pin when the reset is released shall be read in the HEMC\_HECC\_CR0.bitfield3 first and transfer to HEMC\_CR\_NCS0.ECC12\_ENABLE bitfield to avoid any issue later on.

## 10. HECC - HSDRAMC: UNAL Feature

### **Issue**

Several detections of HEMC\_FIX/HEMC\_NOFIX interruptions are visible for the same address of a SDRAM memory when the following conditions are met:

- HSDRAMC\_CFR1.UNAL bit is set
- HECC activated on the HEMC HSDRAMC controller

### **Workaround**

HSDRAMC\_CFR1.UNAL shall be cleared when HECC is enabled for the HEMC HSDRAMC controller.

## 11. Hmatrix: Masters cannot Access Slaves that are Configured with Privilege Access Only

### Issue

The following masters: MCAN0 (M4), MCAN1 (M5), ICM (M11), GMAC (M6), SPW TX (M7), SPW RX (M8), SPW RMAP (M9), IP1553 (M10), add XDMAC (M3 and M12)] cannot access the following slaves: FlexRAM (S0, S1, S7) and DTCM (S6) without removing the permission access (that is, enable user/privilege).

### Workaround

Reduce the size of the protected area in each slave to the minimum size.

Enable the access in read write for each slave.

Examples for slave 6:

- MATRIX0->MATRIX\_PASSR [6]=0x0.
- MATRIX0->MATRIX\_PSR [6]=0xFFFFFFFF;

## 12. ICM HEMC HECC: Incorrect Address Reporting when ICM and HECC Activated Simultaneously

### Issue

When both ICM and HECC are simultaneously monitoring a memory connected to the HEMC controller, the address reported by the HEMC\_HECC\_FAILAR register is not correct (incremented by 0x4).

### Workaround

In this case, correct data at HEMC\_HECC\_FAILAR address and HEMC\_HECC\_FAILAR-0x4 address.

**13. 1553: Interrupt not Triggered in Case of Transmission Without Status Word****Issue**

For transmission without status word, the ETRANS field value is b00. In that case, interrupt is not triggered.

**Workaround**

The interrupts ETX and ERX can be used to monitor the end of transmission; additionally to the ETRANS interrupt, depending on the expected received word status.

## **14. Revision History**

### **14.1 Revision A - January 2020**

This is the initial released version of this document.



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