ATMX150RHA

PLL400MRHA 40 MHz to 450 MHz Programmable PLL

Introduction

PLL400MRHA is a core macro-cell designed for synthesizing and synchronizing a chip clock signal from a reference (internal or external) input clock. The main features are:

- Wide output frequency range (40 MHz to 450 MHz)
- Outputs with different phases (0°, 90°, 180°, and 270°)
- Dedicated power supply rails (vccpll and vsspll)

Table 1. General Characteristics

Parameter	Value
Supply Voltage	1.8V
Placement	Core
Height	575.1 µm
Width	411.5 µm
Area	236654 µm²

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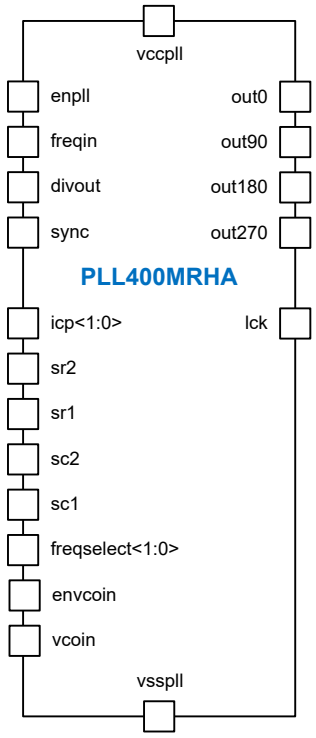
1. Pin Description

The following figure shows the pinout diagram of PLL400MRHA.

Figure 1-1. Pinout Diagram



The following table lists the pins and their functions.

Table 1-1. Pinout

Name	Direction	Related Supply	Description
vccpll	power	NA	Dedicated power supply
vsspll	ground	NA	Dedicated ground supply
enpll	input	vccpll	PLL enable (active-high)
freqselect<1:0>	input	vccpll	VCO frequency range selection bits
icp<1:0>	input	vccpll	Charge Pump current selection bits
sr1	input	vccpll	Internal filter resistance selection bit
sr2	input	vccpll	Internal filter resistance selection bit
sc1	input	vccpll	Internal filter capacitance selection bit
sc2	input	vccpll	Internal filter capacitance selection bit
freqin	input	vccpll	Phase/Frequency reference input
divout	input	vccpll	Phase/Frequency feedback input
out0	output	vccpll	0° phase shift VCO output
out90	output	vccpll	90° phase shift VCO output

.....continued

Name	Direction	Related Supply	Description
out180	output	vccpll	180° phase shift VCO output
out270	output	vccpll	270° phase shift VCO output
lck	output	vccpll	Phase/Frequency lock indicator
envcoin	input	vccpll	VCO external input enable (active-high)
vcoin	input	NA	VCO external input (analog voltage)
sync	input	vccpll	out0 phase lock enable (active-high)

Note: The pins envcoin and vcoin are used to characterize the PLL. When envcoin = ’1’, the analog voltage applied on vcoin must not exceed the power supply voltage of the PLL. In normal mode, envcoin = ’0’, vcoin can be connected to vsspll.
The pin sync enables the out0 Phase Lock mode. The PLL generates the relevant output frequency but locks the phase on out0 instead of that on divout.

2. Operating Modes Description

The following table describes the available functional modes.

Table 2-1. Functional Modes

enpll	envcoin	sync	Description
0	x	x	The PLL is disabled.
1	0	0	The PLL is enabled and in Normal mode.
1	1	0	The PLL is enabled and the pin vcoin is available to control the VCO.
1	0	1	The PLL is enabled and locks the phase on out0.
1	1	1	This is forbidden configuration.

3. Specifications

The following table lists the electrical characteristics of PLL400MRHA.

Table 3-1. Electrical Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
vccpll	Analog power supply		1.65	1.8	1.95	V
T_j	Junction temperature		–55	25	145	°C
F_{in}	Reference input frequency		8		200	MHz
F_{out}	Output frequency		40		450	MHz
Nf	Frequency ratio F_{out}/F_{in}				16	
DC	OVCO output duty cycle		45		55	%
P_{acc}	Phase accuracy	out90 vs out0 or out270 vs out180	–5		5	°
J_{per}	Output period jitter				750	ps
Idd_{on}	ON PLL consumption current	enpll = '1' and max F_{out}			9	mA
Idd_{off}	OFF PLL consumption current	Enpll = '0'			50	µA

Note: Suppose t_n is the sequence of transition times from the output signal and that the nominal period of the reference input signal is T, the output period jitter J_{per} = abs ((t_{n+1} - t_n) - T).
J_{per} varies a lot depending on the PLL configuration. Contact Microchip design centers to get the relevant configuration for your application.

4. Radiation Hardness

The following table lists the parameters of radiation hardness.

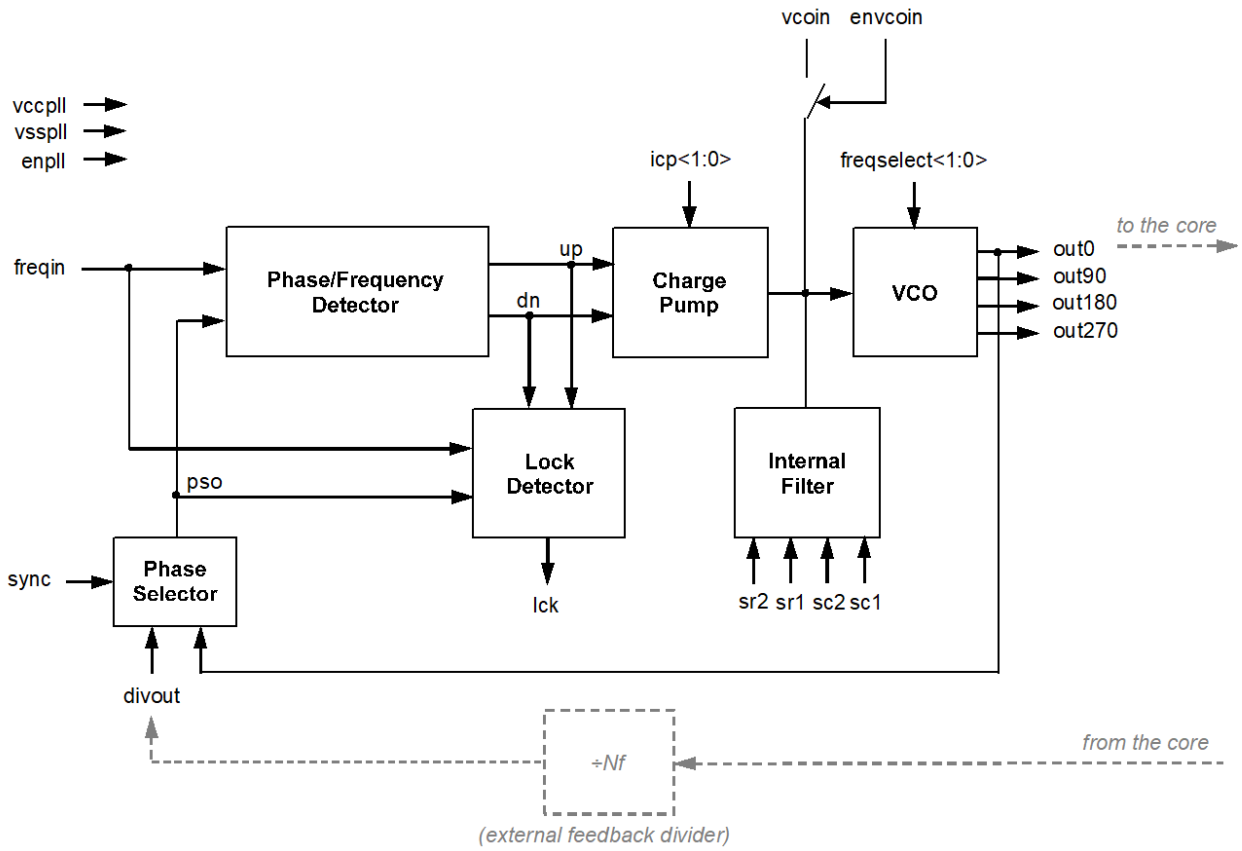
Table 4-1. Radiation Hardness

Parameter	Condition	
TID	ESCC 22900 and Mil-Std 883 TM 1019.5 - 25°C Total dose rate of 300 rad/h	100 kRads (Si) RHA-R (tested 150 kRads (Si))
SEL	ESCC 25100 and JESD57A Input supply voltage vccpll max and Tj = 125°C	> 60 MeV.cm²/mg
SEU	Input supply voltage vccpll min and Tj =25°C	> 30 MeV.cm²/mg

5. Functional Description

The following sections describe the various components of PLL400MRHA.

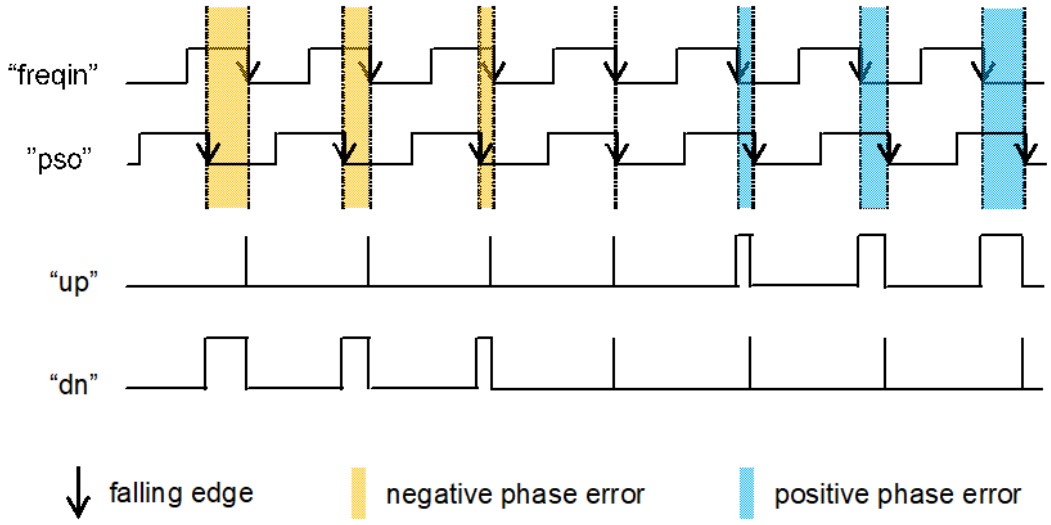
Figure 5-1. Functional Block Diagram



5.1 Phase/Frequency Detector

The Phase/Frequency Detector (PFD) is a digital sequential circuit that detects the phase errors between two signals and converts them into two pulse width modulated signals, “up” and “dn”. Pulses of “up” indicate that the phase errors are positive while pulses of “dn” are generated for negative phase errors. The PFD compares the falling edge of the reference signal on “freqin” with the falling edge of the Phase Selector output signal “pso”.

Figure 5-2. Phase Diagram



5.2 Charge Pump

The charge pump converts the signals “up” and “dn” into positive and negative currents that charge and discharge the PLL internal filter. The positive current increases the VCO input voltage and the output frequency, while the negative current decreases the VCO input voltage and the output frequency. The charge pump current amplitude Icp can be tuned with the selection pins icp<1:0>.

Table 5-1. Charge Pump Truth Table

icp<1:0>	Icp (µA)	
	Min	Max
00	4.5	10
01	6.75	15
10	9	20
11	11.25	25

5.3 VCO

Four VCOs with different frequency ranges and gains are available to generate the output frequencies of the PLL. As per the required output frequencies, a VCO can be selected with appropriate pins freqselect<1:0>.

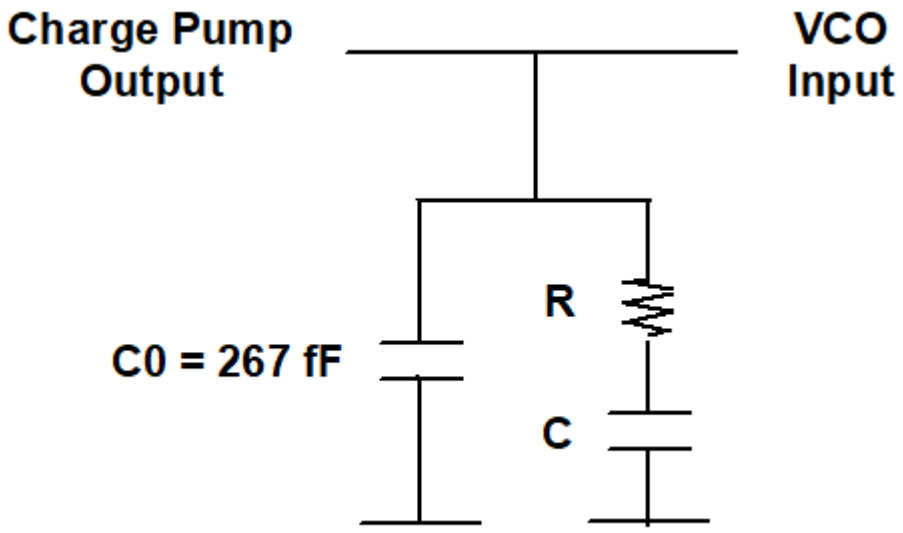
Table 5-2. Frequency Ranges and Gain Variations

freqselect<1:0>	Frequency Range (MHz)		Gain (MHz/V)	
	Minimum	Maximum	Minimum	Maximum
00	40	80	110	160
01	70	150	180	280
10	125	275	300	500
11	250	450	550	1150

5.4 Internal Filter

The internal filter is made up of a built-in capacitor C0 in parallel with a resistor R and a capacitor C in series.

Figure 5-3. Internal Filter



The resistance of R and the capacitance of C depend on the pins sr2, sr1, sc2, and sc1 setting.

Table 5-3. Resistence Options

sr2 sr1	Resistance (kΩ)
00	24
01	6
10	3
11	12

Table 5-4. Capacitance Options

sc2 sc1	Capacitance (pF)
00	20
01	40
10	30
11	60

Notes:

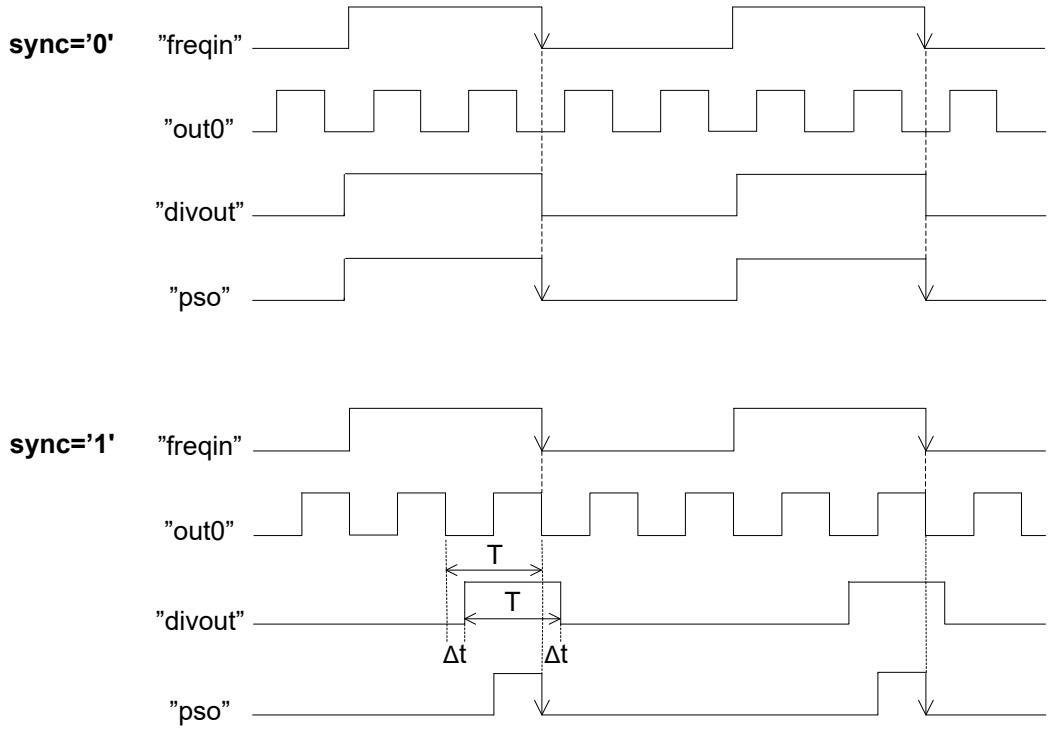
1. Microchip design center determines the relevant PLL configuration, freqselect<1:0>, icp<1:0>, sr2, sr1, sc2, and sc1 setting, according to your application needs. However, several configuration pins like icp<1:0> must be primary inputs of the design in order to better control the performance of the PLL.
2. It is recommended to allow reprogramming the configuration pins to better adjust the PLL stability and reduce its output jitter. For example, the pins icp<1:0> can be primary inputs used to find the best setting and then hard biased on the PCB. If the configuration pins setting is stored in a register, then the latter has to be radiation hardened.

5.4.1 Phase Selector

The phase selector generates the signal “pso”, which is compared with the reference signal “freqin”.

- If sync = ’0’ then “pso” = “divout” → signal phase lock on divout (clock deskewing)
- If sync = ’1’ then “pso” = “out0” and “divout” → signal phase lock on out0 (output phase control)

Figure 5-4. Phase Selector Characteristics



If sync = ’1’, then the external feedback divider is a counter that generates a pulse = ’1’ every Nf periods of “out0”.

It has to be designed according to the following rules:

- The pulse rising and falling edges must be triggered by the falling edges of “out0”.
- The pulse width must be equal to T, the period of “out0”, so, Nf ≥ 2.
- “out0” is not used directly but its buffered one, which is “1 gate delay” late. Let Δt be the feedback divider propagation delay, “1gate delay” ≤ Δt ≤ “1 gate delay” + (T/2).

5.5 Lock Detector

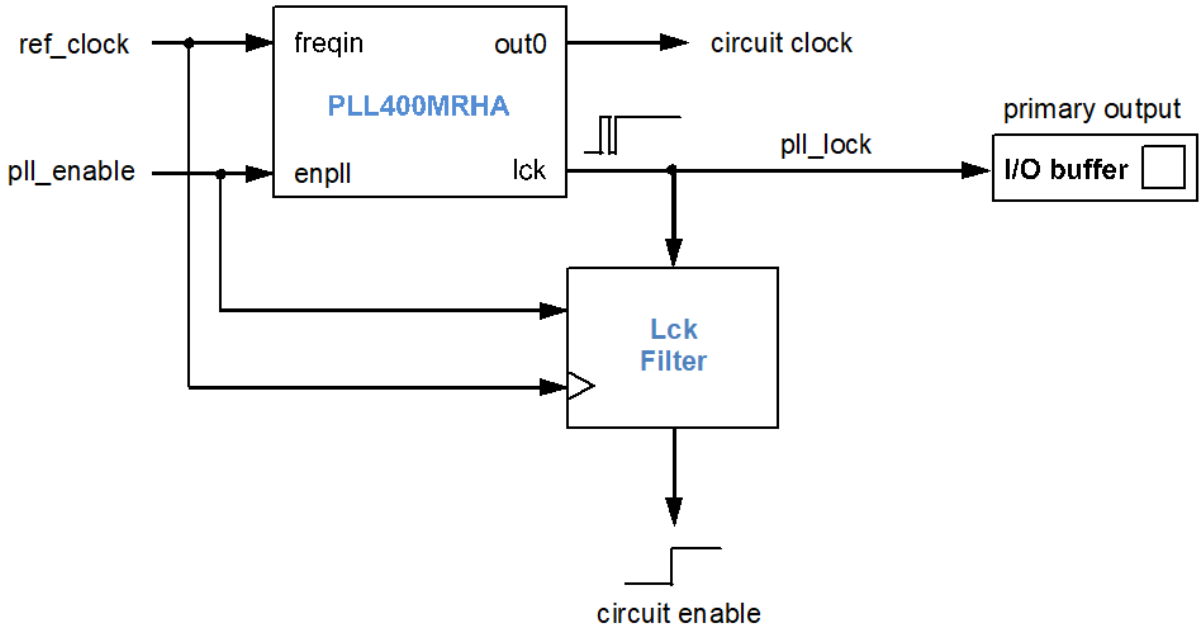
The lock detector indicates if the PLL is Phase/Frequency locked.

- Phase/Frequency locked → lck = ’1’
  When the phase difference between the falling edges of the signals “pso” and “freqin” is lower than half the period of “freqin”, for 12 consecutive periods of “freqin”.
- Phase/Frequency unlocked → lck = ’0’
  As soon as the phase difference between the falling edges of the signals “pso” and “freqin” exceeds half the period of “freqin”.

Note: lck = ’0’ or lck = ’1’ when the PLL is disabled. lck is only reset (lck = ’0’) at PLL startup.

The signal “lck” must not be used directly to enable/disable a circuit. It has to be “filtered”.

Figure 5-5. Lock Detector Circuit



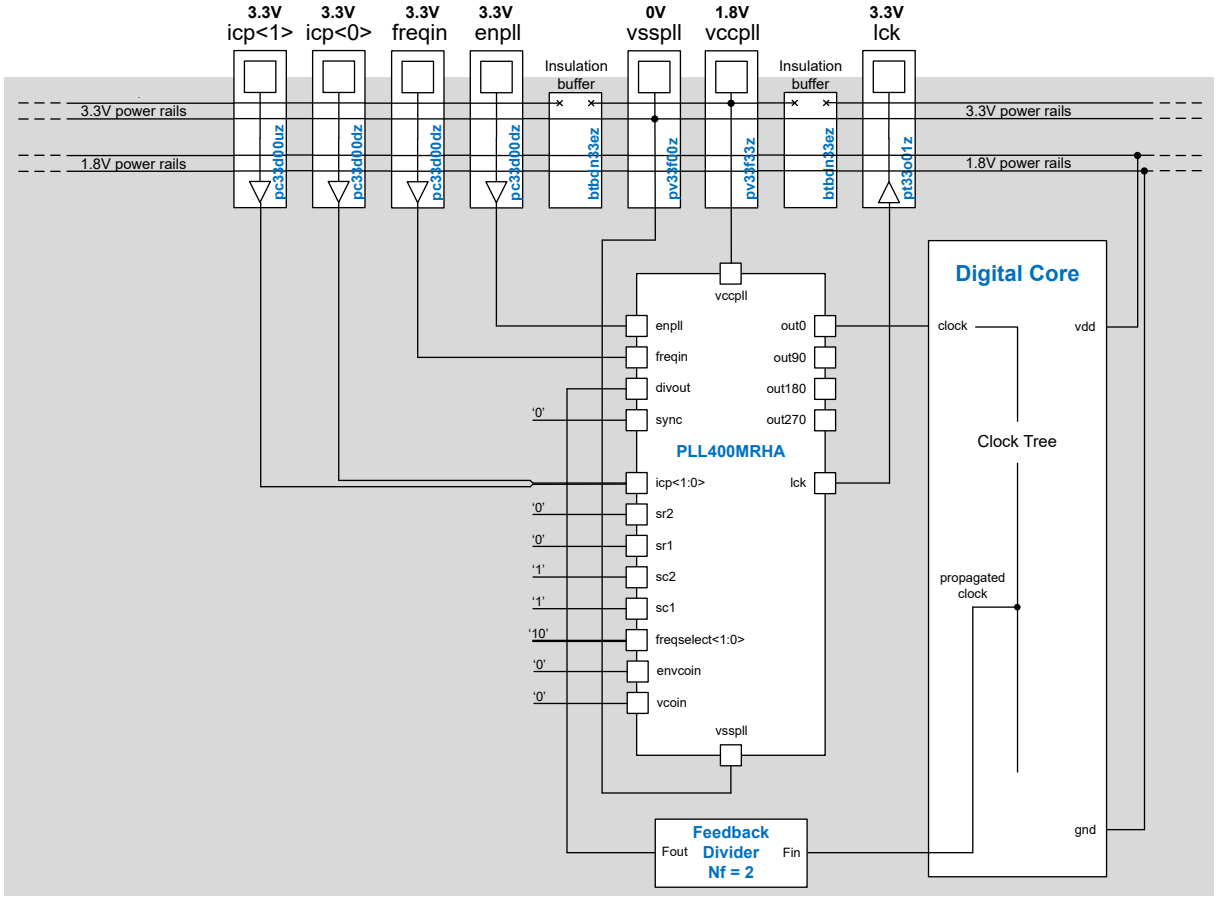
In the above circuit, the PLL lock signal “pll_lock” is propagated to a primary output I/O buffer and is used by the Lck filter to generate a delayed and stable circuit enable signal. The circuit enable signal is reset as soon as pll_enable = ’0’ or pll_lock = ’0’.

Note: Radiation particles or a phase/frequency disruption of the reference signal “freqin” can reset the lock signal (lck = ’0’) while the PLL is still phase/frequency locked. In this case, the PLL has to be restarted to get a correct PLL lock signal again.Once the PLL is Phase/Frequency locked, a disruption of the reference signal “freqin” can reset the PLL lock signal, lck = ’0’ while the PLL is still Phase/Frequency locked. In this case, the PLL has to be restarted to get a correct PLL lock signal again.

5.6 Typical Application

In this typical application, PLL400MRHA generates a clock signal for the digital core. The clock signal on out0 is propagated in the clock tree of the digital core, then its frequency is divided by Nf = 2 and the resulting signal on divout is compared with the reference signal on freqin. When the PLL is Phase/Frequency locked, the frequency of the propagated clock signal, in the digital core, is twice higher than that of the reference one and its falling edges are in phase with those of the reference one. The lock signal of the PLL on lck is propagated to a primary output. The behavior of the PLL can slightly change in setting the input pins icp<0> and icp<1>. Thus, the phase/frequency lock time and the output signal jitter can be reduced.

Figure 5-6. Typical Application Circuit



6. Testability Requirements

Unless otherwise specified at the DSR, the lock is to be checked and Fout, the output frequency parameters, is to be measured.

For these tests:

- The external feedback divider must be connected to the PLL and should be enabled before the PLL startup.
- The reference signal on freqin must be compliant with the PLL specifications.
- The relevant PLL configuration must be given by a Microchip design center.
- The lock signal on lck must be propagated to a primary output to assess the PLL lock.

The PLL must be Phase/Frequency locked in less than 100 µs.

It is recommended to measure the PLL output frequency to confirm that the PLL is Phase/Frequency locked. So, the PLL output signal on out0 can also be propagated to a primary output in order to extract the PLL output frequency, the duty cycle, and the jitter. If the signal frequency is too high (>100 MHz) for a digital output buffer or too high (>320 MHz) for a LVDS buffer then its frequency has to be divided before being propagated.

7. Integration Guidelines

The following sections provide guidelines for efficient sytem integration.

7.1 Placement and General Rules

The PLL is a noisy and sensitive circuit that has to be placed far from the digital core and other analog blocks. It has to be close to the I/O buffers it is connected to and the wires used to connect the PLL must be as wide as its corresponding pins.

The PLL does not include the feedback divider. It must be placed near the PLL but without disturbing each other.

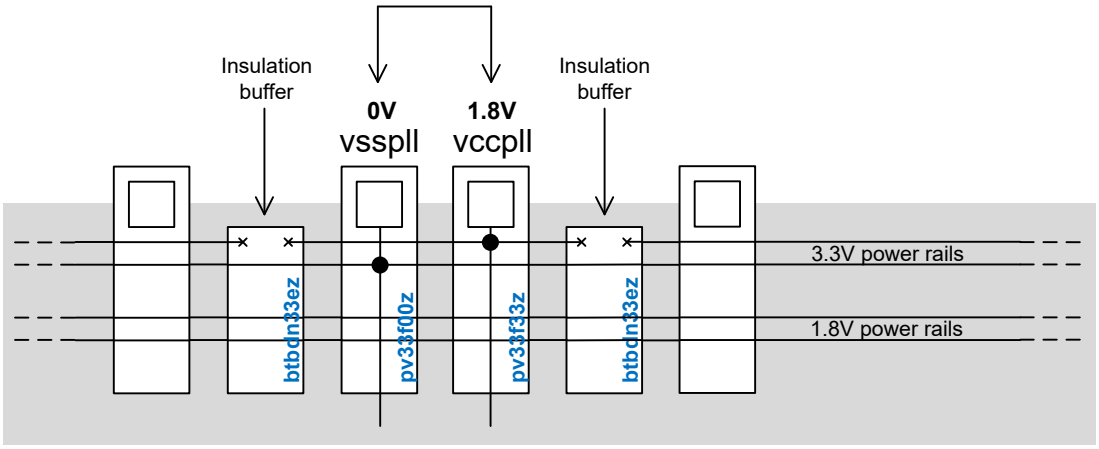
Configuration pins should be primary inputs of the design to better control the stability and the performance of the PLL. At least, icp<1:0> should be reprogrammable. If the configuration pins setting is stored in a register then the latter has to be radiation hardened.

7.2 Supplies Routing and Decoupling

The PLL has its own power supply pins, vccpll, and vsspll. They are connected to specific power supply buffers which are separated from the others by insulation buffers. The routing resistances between the pins of the power supply/ground buffers and the power supply/ground pins of the PLL must not be higher than 5 Ω. To reduce the noise coupling, vccpll should be connected to a dedicated package cavity_pad/lead.

- Ground buffer for vsspll - pv33f00z
- Power supply buffer for vccpll - pv33f33z
- Insulation buffer - btbdn33ez

Figure 7-1. Ground and Power Supply Buffers



Note: Unless otherwise noted, all the power supplies must be decoupled externally with large capacitors, 1 uF//10 nF.

7.3 Analog Signals Routing

The analog signal vcoins must be routed to have less than 51 Ω resistance, from the source to the sink.

The signal routed to the pin vcoin is an analog voltage and all digital or clock signals must be routed with 1 µm spacing away from this signal. In case of crossing digital or clock signals, a shield connected to the analog ground is required between the noisy net and the analog signal.

If these conditions are not met, contact the design group Microchip design centers to investigate potential performance impact.

7.4 Routing Constraints

The following table lists the routing constraints for PLL400MRHA.

Table 7-1. Routing Constraints

Pin Name	Signal Type	Related Power Supply	Max DC Current Flowing (mA)	Max allowed Routing Resistance (Ω)	Max Allowed Capacitance to Ground (pF)	Other Constraints
vccpll	Supply	-	9	5	-	Star routing to power supply.
vsspll	Ground	-	-	5	-	Star routing to ground.
enpll	Digital	vccpll	-	-	-	
freqselect<1:0>	Digital	vccpll	-	-	-	
icp<1:0>	Digital	vccpll	-	-	-	
sr1	Digital	vccpll	-	-	-	
sr2	Digital	vccpll	-	-	-	
sc1	Digital	vccpll	-	-	-	
sc2	Digital	vccpll	-	-	-	
freqin	Digital	vccpll	-	-	-	
divout	Digital	vccpll	-	-	-	
out0	Digital	vccpll	-	-	-	
out90	Digital	vccpll	-	-	-	
out180	Digital	vccpll	-	-	-	
out270	Digital	vccpll	-	-	-	
lck	Digital	vccpll	-	-	-	
envcoin	Digital	vccpll	-	-	-	
vcoin	Analog	-	-	5	-	No crossing with other signals, otherwise, shielding to vsspll. 1 µm minimum spacing from other signals.
sync	Digital	vccpll	-	-	-	

8. Revision History

Revision	Date	Description
A	September 2020	The following is a summary of changes in revision A of this document. • Updated the document as per Microchip standards. • Modified the radiation tolerance specifications.

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