ATMX150RHA

OSCRC10MRHA 4/8/10/12 MHz Programmable RC Oscillator

Introduction

OSCRC10MRHA is a programmable RC oscillator, which generates a 4/8/10 or 12 MHz typical frequency clock signal. Frequency accuracy of ±10% is achieved over supply voltage and temperature range.

The oscillation frequency is a stable 6 µs after start up as a maximum.

Table 1. Parameters and Values

Parameter	Value
Supply voltage	1.8V
Placement	Core
Height	420 µm
Width	240.8 µm

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1. Pin Description

The following figure and table explain the pin details of OSCRC10MRHA.

Figure 1-1. Pinout Diagram

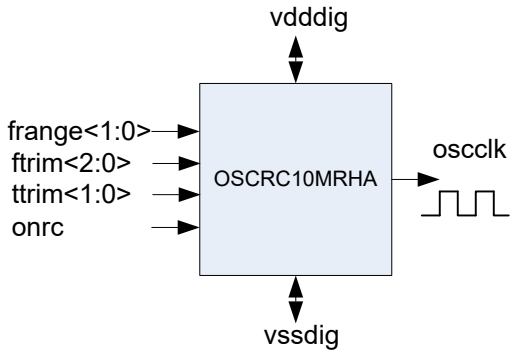


Table 1-1. Pin Description

Pin name	I/O	Function	Fanin/Fanout (pF)
oscclk	Output	Clock At high level when ONRC = 0	1
frange<1:0>	Input	Output clock frequency selection bits	0.04
ftrim<2:0>	Input	Trimming bits **(for test purpose only)** Can be left unconnected	—
ttrim<1:0>	Input	Temperature tuning bits **(for test purpose only).** Can be left unconnected	—
ONRC	Input	Oscillator enable when ONRC = 1	0.03
VDDDIG	—	Power supply	—
VDDDIG	—	Analog ground supply	—

2. Specifications

Junction temperature range is, Tj = (–55 ºC to 145 ºC), over whole voltage and process variation, unless otherwise noted.

Table 2-1. Specifications

Parameter		Conditions	Min	Type	Max	Unit
VDDDIG	Supply voltage		1.65	1.8	1.95	V
F0	Nominal Frequency	frange<1:0> = 0b00 default trim (1)	3.6	4	4.4	MHz
		frange <1:0> = 0b01 default trim (1)	7.2	8	8.8	
		frange <1:0> = 0b10 default trim (1)	9	10	11	
		frange <1:0> = 0b11 default trim (1)	10.8	12	13.2	
Duty	Duty cycle		47	50	53	%
Idd_{on}	Power consumption	After startup time			750	µA
T_{on}	Startup time				6	µs
Idd_{stby}	Standby consumption	onrc = 0			0.2	µA

Note:

1. Ttrim <1:0> = 0b11 and Ftrim <2:0> = 0b011

3. Radiation Hardness

The following table lists the radiation hardness details of OSCRC10MRHA.

Table 3-1. Radiation Hardness

Parameter	Conditions	
TID	ESCC22900 and Mil-Std 883 TM 1019 Input supply voltage V_{DD} max, Tj = 25 °C and total dose rate of 300 rad/h	100 kRads (Si) RHA (Tested at 150 kRads (Si))
SEL	ESCC 25100 and JESD57A Input supply voltage V_{DD} max and Tj = 125 °C	> 60 MeV.cm²/mg
SEU	Input supply voltage V_{DD} min and Tj = 25 °C	> 60 MeV.cm²/mg

4. Functional Description

The following table lists the values that are obtained for a junction temperature between –55 °C and 145 °C and for a power supply between 1.65V and 1.95V.

Table 4-1. Functional Description

onrc	frange<1:0>	oscclk
L	XX	L
H	00	4 MHz ±10%
H	01	8 MHz ±10%
H	10	10 MHz ±10%
H	11	12 MHz ±10%

5. Trimming Procedure

The output frequency can be fine-tuned. The following bits are available for the trimming purpose:

- ttrim <1:0> setup impact frequency temperature coefficient. Default setup is equivalent to ttrim <1:0> = 0b11.
- ftrim <2:0> setup impact absolute frequency value. Default setup is equivalent to ftrim <2:0> = 0b011.

Perform the following steps:

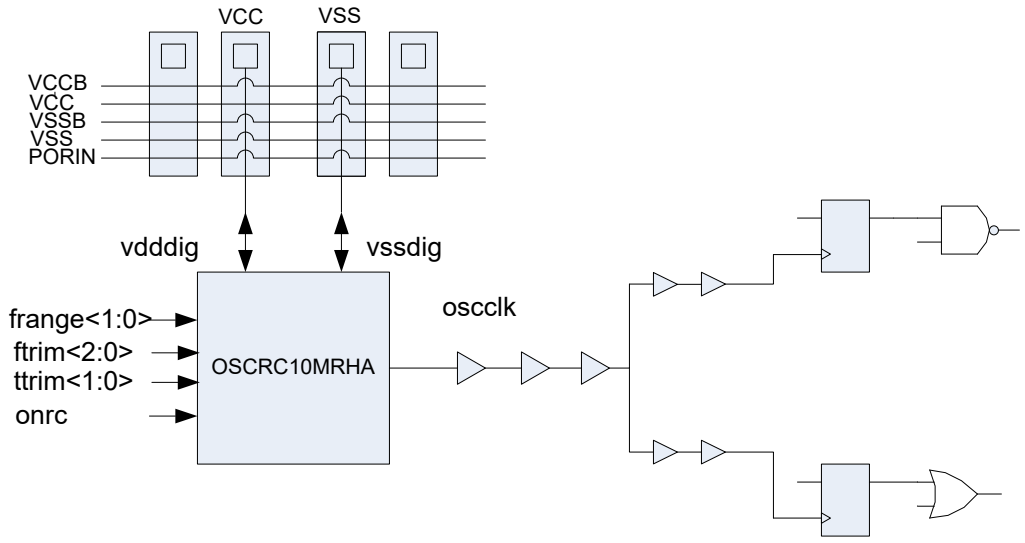
1. Find the compensation in temperature with ttrim, with at least two points. It has been demonstrated that the best value is 0b11.
2. Apply 25 °C and tune the frequency value with ftrim.
3. Irrespective of the frequency range, the ttrim and ftrim bits have the same value.

Note: The trimming signals cannot be left unconnected.

6. Typical Application

- V_{CC} : pv33i18z
- V_{SS} : pv33i00z

Figure 6-1. Typical Application



7. Testability Requirements

Unless otherwise specified at the DSR, the F0 parameter is to be measured.

For this test, the oscclk pin must be accessible through a primary I/O.

8. Integration Guidelines

The following sections detail the integration guidelines.

8.1 Placement and General Rules

- The wires used to connect the cell must have the width equal to the pin width.
- As this cell can induce noise, it must be placed far from the sensitive cells.

8.2 Power Supplies

- The wires that connect the cell must have the width equal to the pin width.
- Power supplies and ground must be star routed.
- The power supplies must be externally decoupled with capacitors 1 µF//100 nF as close as possible to the package.

8.3 Output Signal

The output signal is noisy and must be routed far from the sensitive node to not induce perturbation.

8.4 Routing Constraints

The following table lists the routing constraints details.

Table 8-1. Routing Constraints

Pin Name	Signal Type	Max DC current flowing (mA)	Max Allowed Routing Resistance (Ω)	Other Constraints
vdddig	Supply	0.75	30	Star routed to the power supply input
vssdig	Supply	0.75	30	Star routed to the power supply input
onrc	Digital	—	—	—
frange<1:0>	Digital	—	—	—
ftrim<2:0>	Digital	—	—	—
ttrim<1:0>	Digital	—	—	—
oscclk	Clock	—	—	Clock signal must be routed with 1 µm to any other signal

9. Revision History

Revision	Date	Description
A	September 2020	The following is a summary of changes in revision A of this document. • Updated the document as per Microchip standards. • Modified the radiation tolerance specifications.

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