
MUX8RHA 8-Channel Analog Multiplexer

Introduction

MUX8RHA is a 8-channel, digitally controlled, analog multiplexer. It is power supplied with vdddig (1.8V or 3.3V) for its control part and vddana (3.3V) for its internal switches. The analog input voltages, on the pins ai33in0, ai33in1...7 can vary from 0V to vddana.

Table 1. Parameters and Values

Parameter	Value
Supply voltages	1.8V or 3.3V (vdddig) 3.3V (vddana)
Placement	Core
Height	291.2 μm
Width	100.8 μm

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1. Pin Description

The following figure and table explains the pin details of MUX8RHA.

Figure 1-1. Pinout Diagram

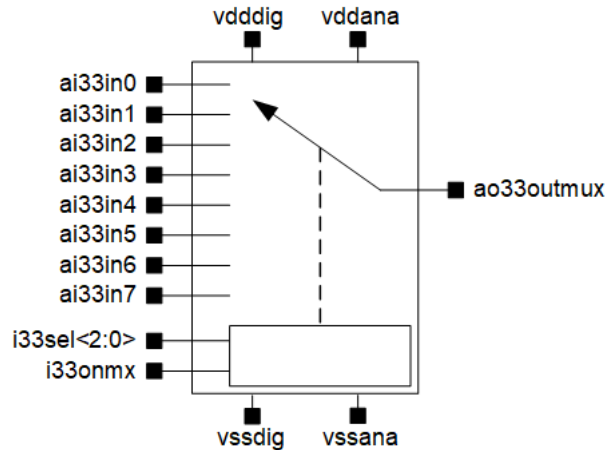


Table 1-1. Pin Descriptions

Name	Direction	Related Supply	Description	Fanin/Fanout
vdddig	power	NA	Digital 1.8V or 3.3V power supply (equal to the core supply voltage)	NA
vssdig	ground	NA	Digital ground	NA
vddana	power	NA	Analog 3.3V power supply	NA
vssana	ground	NA	Analog ground	NA
ai33in0...7	input	vddana	Analog inputs	See the equivalent circuits on ON and OFF Channel Equivalent Circuits .
i33sel<2:0>	input	vdddig	Channel selection pins	0.03 pF
i33onmx	input	vdddig	Active high MUX enable	0.03 pF
ao33outmux	output	vddana	Analog output	See the equivalent circuits on ON and OFF Channel Equivalent Circuits .

2. Functional Description

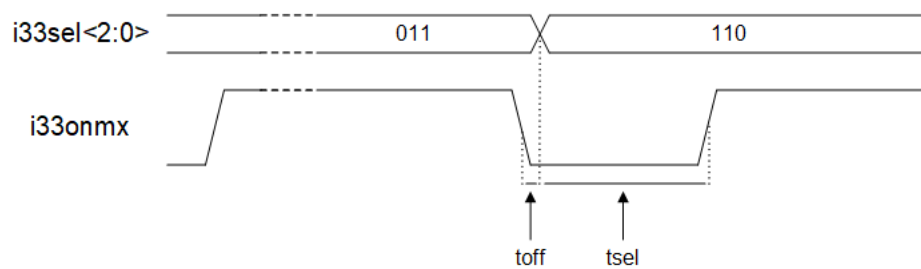
The following table lists the truth table details.

Table 2-1. Truth Table

i33onmx	i33sel<2:0>	ON Channel
0	xxx	NONE
1	000	ai33in0
1	001	ai33in1
1	010	ai33in2
1	011	ai33in3
1	100	ai33in4
1	101	ai33in5
1	110	ai33in6
1	111	ai33in7

To avoid channel shortcuts, it is recommended to select the ON channel when i33onmx = 0.

Figure 2-1. Timing Diagram



min toff = 1 ns

min tsel = 9 ns

3. Specifications

Junction temperature is $T_j = (-55\text{ }^{\circ}\text{C to } 145\text{ }^{\circ}\text{C})$, worst cases of power supply voltage and process unless otherwise noted.

The following table lists the specifications of the analog multiplexer MUX8RHA alone, without its PnR parasitics, primary I/O buffers, package, and board environment (important to consider in extracting the parameters from measurements).

Table 3-1. Specifications

Code	Parameter	Conditions	Min	Type	Max	Unit	
vdddig	Digital power supply voltage	1.8V voltage range	1.65	1.8	1.95	V	
		3.3V voltage range	3.0	3.3	3.6		
vddana	Analog power supply voltage	3.3V voltage range	3.0	3.3	3.6	V	
Ipeak	Peak current on vddana	vddana = 3.6V, vdddig = 1.95V	—	7.3	7.6	$\mu\text{A}/\text{MHz}$	
Ron ⁽⁵⁾	Switch ON resistance	vddana = 3.0V, vdddig = 1.65V	—	66	143	Ω	
Canon ⁽⁵⁾	Analog input capacitance	See the equivalent circuits are on ON and OFF Channel Equivalent Circuits .	—	207	264	fF	
Cotton ⁽⁵⁾	Analog output capacitance	See the equivalent circuits are on ON and OFF Channel Equivalent Circuits .	—	863	916	fF	
Snout ⁽⁵⁾	Coupling capacitance	See the equivalent circuits on ON and OFF Channel Equivalent Circuits .	—	—	24	fF	
Cinoff ⁽⁵⁾	Analog input capacitance	See the equivalent circuits on ON and OFF Channel Equivalent Circuits .	—	—	91	fF	
Coutoff ⁽⁵⁾	Analog output capacitance	See the equivalent circuits on ON and OFF Channel Equivalent Circuits .	—	—	787	fF	
Di ⁽⁵⁾	Signal distortion ⁽¹⁾	Sine wave signal Co = 10 pF, vddana = 3V	Fi = 200 KHz	—	—	0.03	%
			Fi = 100 KHz			0.02	
Ct ⁽⁵⁾	Crosstalk between any two channels ⁽²⁾	Ri = 50 Ω , Ci = 5 pF	10 MHz	—	—	-85	dB
			1 MHz			-105	
		Ri = 1 k Ω , Ci = 5 pF	10 MHz	—	—	-60	dB
			1 MHz			-80	
Iso ⁽⁵⁾	OFF channel input/output isolation ⁽³⁾	Ro = 2.5 k Ω , Co = 5 pF	10 MHz	—	—	-60	dB
			1 MHz			-80	
Idd	Standby current	i33onmx = 0	—	—	1	μA	

ATMX150RHA

Specifications

.....continued

Code	Parameter	Conditions	Min	Type	Max	Unit
I _{max}	Channel max current allowed to avoid electromigration	DC current ⁽⁴⁾	—	—	6	mA
PSRR	Power Supply Rejection Ratio	Noise on vddana	10 MHz 1 MHz 1 KHz 1 Hz	—	—35 —55 —115 —115	dB
t _{off}	Time to disable all the channels	—	—	1	—	ns
t _{sel}	Time to activate a channel	—	—	9	—	ns

Notes:

1. A sine wave of frequency F_i is injected in the selected channel. The sine wave amplitude is rail to rail and the output $ao33outmux$ is loaded with C_o .
2. One channel is ON while the others are OFF with their inputs connected to $R_i//C_i$.
3. The channel is OFF with its output $ao33outmux$ connected to $R_o//C_o$.
4. A peak current of 18 mA is allowed on a channel.
5. The values that are given are not production-tested values. Normally, they are typical values, considering the MUX8RHA design only, given for the benefit of the designer. These values are impacted by the IP integration and must consider routing, die bonding, packaging, and board design.

Figure 3-1. ON and OFF Channel Equivalent Circuits

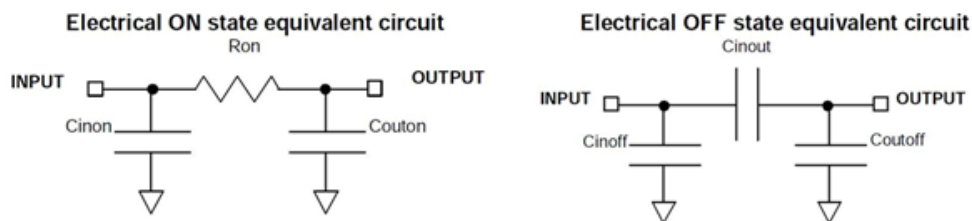
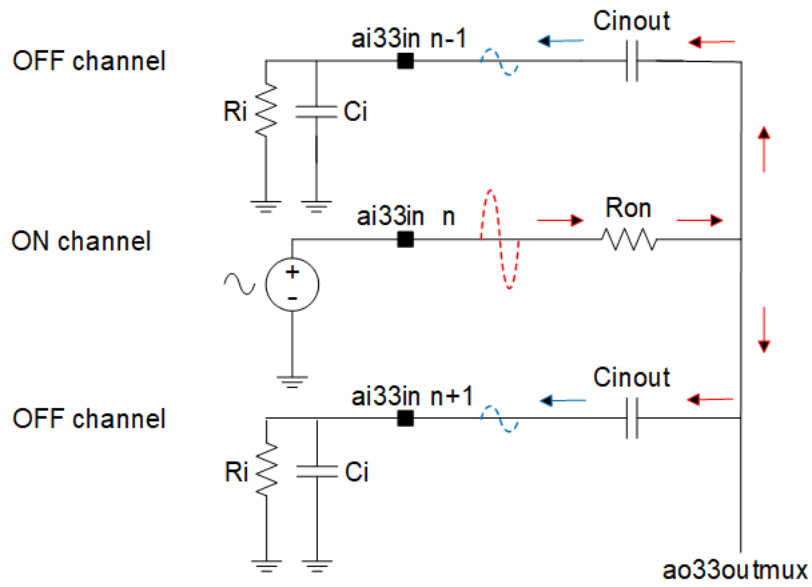


Figure 3-2. Crosstalk Ct Measurement



4. Radiation Hardness

The following table lists the radiation hardness details.

Table 4-1. Radiation Hardness

Parameter	Conditions	
TID	ESCC22900 & Mil-Std 883 TM 1019 Input supply voltage vddana and vddig min, Tj = 25 °C, total dose rate of 300 rad/h	100 kRads (Si) RHA-R (tested 150 kRads (Si))
SEL	ESCC 25100 & JESD57A Input supply voltage vddana and vddig max and Tj = 125 °C	> 60 MeV.cm ² /mg
SEU	Input supply voltage vddana and vddig min and Tj = 25 °C	> 30 MeV.cm ² /mg

5. Typical Application

The following figure shows the typical application details.

Figure 5-1. Multiplexing Analog Inputs to an ADC



6. Testability Requirements

Unless otherwise specified at the DSR, the analog multiplexer MUX8RHA must be tested at an appropriate speed to evaluate its performances according to the analog input signal voltage range and frequency.

7. Integration Guidelines

The following sections describe more about the integration guidelines.

7.1 Placement and General Rules

Wires used to connect the analog multiplexer must have the width equal to the pin width. Wires for analog signals must be as short as possible to reduce the electromagnetic coupling (crosstalk). Otherwise, analog signals must be routed with shielded lines.

7.2 Analog Input Signals

The RLC parasitic coming from the analog input signal routing must be minimized. They depend on several layout parameters like the routing metal layer, the wire width and length, and the spacing from other signals.

7.3 Power Supply Decoupling

All power and ground pads must be connected to large decoupling capacitors.

7.4 Routing Constraints

The following table lists the routing constraints details.

Table 7-1. Routing Constraints

Pin name	Signal Type	Related Power Supply	Max DC Current Allowed (mA)	Max Allowed Routing Resistance (Ω)	Max Allowed Capacitance to Ground (pF)	Other Constraints
vdddig	Digital power	—	—	—	—	—
vssdig	Digital ground	—	—	—	—	—
vddana	Analog power	—	—	—	—	—
vssana	Analog ground	—	—	—	—	—
ai33in0...7	Analog input	vddana	6	—	—	1 μm minimum spacing between two adjacent analog inputs and from other signals
i33sel<2:0>	Digital input	vdddig	—	—	—	—
i33onmx	Digital input	vdddig	—	—	—	—
ao33outmux	Analog output	vddana	6	—	—	1 μm minimum spacing from other signals

8. Revision History

Revision	Date	Description
A	September 2020	The following is a summary of changes in revision A of this document. <ul style="list-style-type: none">• Updated the document as per Microchip standards.• Modified the radiation tolerance specifications.

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