AT7991

Rad-Hard GNSS Baseband Processor

General Description

The AT7991, also known as the AGGA-4 developed under ESA contract and the successor of the AGGA-2 chip, is a highly integrated, GNSS base-band processor with 32-bit SPARC V8 embedded general purpose processor, and various peripherals.

The GNSS processing unit comprising front-end modules pre-processes digital near-baseband sample streams from four GNSS antennas, as well as 36 single-frequency GNSS correlation channels. Each channel comprises final down-conversion with carrier NCO, as well as a de-spreader unit with a code generator unit, code delay lines, and a set of 2×5 correlators. The very flexible code generator allows generating a large variety of replica GNSS spreading codes for multiple constellations (Galileo, GPS, Glonass, Beidou). The channels also include carrier and code aiding units, computing parametrizable second order updates to the carrier, and code NCO's, which helps reducing the SW loop update rate, hence facilitating the tracking of multiple signals in a highly dynamic environment.

Besides the GNSS unit, the AT7991 includes European Space Agency (ESA) SPARC V8 LEON2 fault-tolerant general purpose microprocessor with a Cobham Gaisler GRFPU IEEE754 Floating Point Unit.

The System-On-Chip (SoC) is completed by a large set of peripherals, namely a 128-point FFT module, a CRC unit, and various communication links for example, SpaceWire, MIL STD 1553, SPI, UART, and GPIOs. Some of them have DMA capability.

With its GNSS unit and the general space-oriented SoC architecture, the AT7991 is suitable for a large variety of navigation-related space applications.

The processor is manufactured using the Microchip’s 0.18 µm rad-hard ATC18RHA CMOS technology.

Features

- SPARC V8 High Performance Low-power 32-bit processor core
- – AT697F Sparc V8 processor
  – Integrates LEON2-FT 1.0.9.16.2 IP Core
  – 8-Register Windows
  – Advanced Architecture
  – • 5-Stage Pipeline
    • 32-Kbytes 4-way associative instruction cache
    • 16-Kbytes 2-way associative data cache
- Integrated 32/64-bit IEEE 754 Floating-point Unit
- Flexible Memory Interface
  – PROM Controller
  – SRAM Controller
- RAM write protection Unit
- Interrupt Controllers
- General Purpose Interface
  – 32 Parallel I/O Interface
  – One serial output with 16-bytes FIFO
- Timers

  - Four 32-bit Timers
  - One 10-bit prescaler
  - Watchdog Timer
- Two 8-bit UARTs
  - DMA capabilities
- One SPI interface
- SpaceWire interface
  - 4 single-ended interfaces
  - DMA capabilities
  - Data rate up to 87 Mbits/sec
- Global Navigation Satellite System (GNSS)
  - Front-end with four scalable input modules that can be connected to multiple antennas and supports digital down-conversion, beam-forming, and enhanced power level detection
  - 36 highly configurable single-frequency/double code GNSS channels
  - Code and carrier loop aiding support, and optimized raw sampling for open-loop signal tracking
- MIL STD 1553B interface
  - Compliant to MIL-STD-1553BB standard
  - Bus Controller and Remote Terminal configurations available
  - 1553 data rate: 1 Mbits/sec
- On-chip configurable CRC module to support multiple standards
- On-chip 128-point fixed-point in/floating point output FFT module
- Embedded EEPROM power ON/OFF functionality
- Debug and Test Facilities
  - Debug Support Unit (DSU) for Trace and Debug
  - Debug Support Links (DCL): available: UART or SpaceWire
  - Hardware watchpoints
  - Debug pins at various points of the GNSS processing chain
- Operating range
  - Voltages
    - 3.3 V +/- 0.30 V for I/O
    - 1.8 V +/- 0.15 V for Core
  - Temperature
    - -55 °C to 125 °C
- Clocks
  - System clock : up to 87 MHz
  - Two on-chip PLLs and on-chip dividers
- Package MQFP352
- Radiation performances
  - RHA capability of 100 krad (Si) according to the MIL-STD-883 method 1019.
  - No single event latch up below a LET threshold of 65 MeV.cm2/mg at 125 °C

References

- [1] : AT7991 User Manual – [41097]
- [2] : SPARC V8 Architecture Manual – version 8 – (rev. SAV080SI9308)
- [3] : AMBA standard – rev 2.0 [ARM IHI 0011A]

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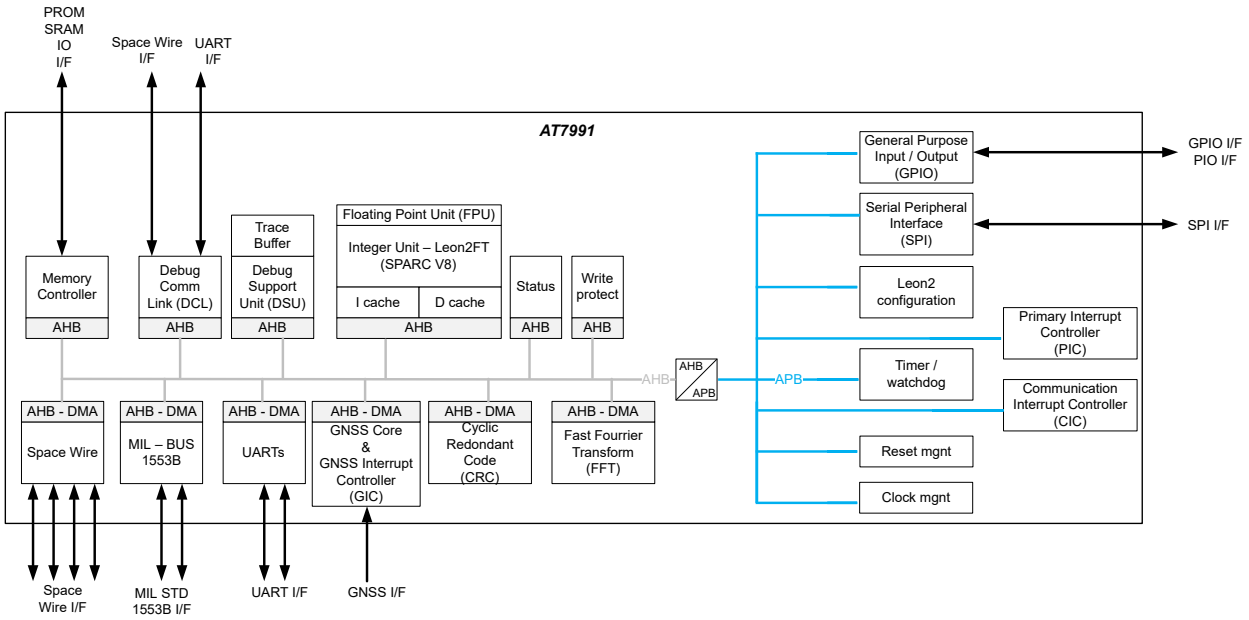
1. Block Diagram

The following block diagram gives an overview of the AT7991 product.

Figure 1-1. AT7991 Block Diagram



2. Signal Description

The following table gives details on signal names classified by peripheral.

Table 2-1. Signals Description

Signal Name	Function Definition	Direction	Active Level	Comments
SYSTEM, RESET, ERROR				
AT7991_RESET_N	AT7991 reset input signal	(Input)	Low	—
PWR_ON_RESET_N	Power on reset input signal	(Input)	Low	—
GNSS_RESET_N	GNSS reset input signal	(Input)	Low	—
MIL_RESET_OUT_N	MIL STD 1553B - reset input signal	(tri-state Output)	Low	External pull up shall be applied on this pin.
NMI_EXT	Non maskable input signal	(Input)	rising edge	—
ERROR_N	Error signal	(tri-state Output)	Low	External pull up shall be applied on this pin.
WDOG_RST_N	Watchdog reset signal	(tri-state Output)	Low	External pull up shall be applied on this pin.
WDOG_N	Watchdog timeout signal	(tri-state Output)	Low	External pull up shall be applied on this pin.
CLOCKS and PLL				
SYS_PLL_FREQSEL[1:0]	System pll frequence output selector signal	(Input with pull down)	—	
SYS_CLK_DIV[3:0]	System clock - divider ratio selector signal	(Input with pull up)	—	—
SYS_PLL_BYPASS	System clock - system pll bypass signal	(Input)	High	—
EXT_SYS_CLK	System clock input signal	(Input)	—	—
SYS_PLL_LOCK	System clock pll lock signal	(Output)	High	—
SYS_CLK_OUT	(System clock/10) feedback signal	(Output)	-	—
MIL_PLL_LOCK	MIL STD 1553B clock pll lock signal	(Output)	High	—
EXT_MIL_CLK	MIL STD 1553B pll input signal	(Input)	—	—
MIL_CLK_OUT	(MIL STD 1553B clock /4) feedback signal	(Output)	—	—
EXT_CORE_CLK	GNSS - CoreClock signal	(Input)	—	—
HALF_SAMPLE_CLK	GNSS - half sample clock signal	(Input)	—	—
EXT_CLK	GNSS - external clock counter signal	(Input)	—	—

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Signal Name	Function Definition	Direction	Active Level	Comments
EXTERNAL MEMORY INTERFACE				
ADDRESS[27:0]	Common address bus signal	(Output)	—	—
DATA[31:0]	Common data signal	(Input/Output)	—	—
CB[6:0]	Common check bit signal	(Input/Output)	—	—
RAMS_N[4:0]	RAM chip select signal	(Output)	Low	—
ROMS_N[1:0]	ROM chip select signal	(Output)	Low	—
RAMOE_N[1:0]	RAM output enable signal	(Output)	Low	—
RWE_N[3:0]	ROM and RAM byte write enable signal	(Output)	Low	—
IOS_N	IO chip select signal	(Output)	Low	—
OE_N	ROM and IO output enable signal	(Output)	Low	—
WRITE_N	ROM and IO write enable signal	(Output)	Low	—
BEXC_N	Common bus exception signal	(Input)	Low	—
BRDY_N	Common bus ready signal	(Input)	Low	—
READ	ROM and IO read enable signal	(Output)	High	—
INPUT/OUTPUT INTERFACE				
GPIO[15:0]	General purpose input output signals	(Input/Output)	—	—
PIO[15:0]	General purpose input output signals	(Input/Output)	—	—
SGPO	Serial general purpose output signal	(Output)	—	—
SPACEWIRE (SPW)				
SPW_RX_D[3:0]	SpaceWire - receiver data signals	(Input)	—	—
SPW_RX_S[3:0]	SpaceWire - receiver strobe signals	(Input)	—	—
SPW_TX_D[3:0]	SpaceWire - transmitter data signals	(Output)	—	—
SPW_TX_S[3:0]	SpaceWire - transmitter strobe signals	(Output)	—	—
MIL STD 1553B				
MIL_RX0	MIL STD 1553B - receiver primary signal	(Input)	—	—
MIL_RX0B	MIL STD 1553B - receiver redundant signal	(Input)	—	—
MIL_TX0	MIL STD 1553B - transmitter primary signal	(Output)	—	—

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Signal Name	Function Definition	Direction	Active Level	Comments
MIL_TX0B	MIL STD 1553B - transmitter redundant signal	(Output)	—	—
MIL_TX0INH	MIL STD 1553B - transmitter inhibit signal	(Output)	High	—
MIL_RX1	MIL STD 1553B - receiver primary signal	(Input)	—	—
MIL_RX1B	MIL STD 1553B - receiver redundant signal	(Input)	—	—
MIL_TX1	MIL STD 1553B - transmitter primary signal	(Output)	—	—
MIL_TX1B	MIL STD 1553B - transmitter redundant signal	(Output)	—	—
MIL_TX1INH	MIL STD 1553B - transmitter inhibit signal	(Output)	High	—
GLOBAL NAVIGATION SATELLITE SYSTEM (GNSS)				
ASEO	GNSS - Antenna switch epoch output signal	(Output)	High	—
ASEI	GNSS - Antenna switch epoch input signal	(Input)	High	—
MEO	GNSS - measurement epoch output signal	(Output)	High	—
MEI	GNSS - Measurement epoch input signal	(Input)	High	—
PPSO	GNSS - Pulse per second output signal	(Output)	High	—
PPSI	GNSS - Pulse per second input signal	(Input)	High	—
AU_TRIGGER	GNSS - Aiding unit trigger signal	(Input)	High	—
IMT_12	GNSS - Instrument measurement time signal	(Output)	High	—
ASC[1:0]	GNSS - Antenna switch controller signal	(Output)	—	—
INPUT_A0[2:0]	GNSS - input A signal	(Input)	—	—
INPUT_A1[2:0]	GNSS - input A signal	(Input)	—	—
INPUT_A2[2:0]	GNSS - input A signal	(Input)	—	—
INPUT_A3[2:0]	GNSS - input A signal	(Input)	—	—
INPUT_B0[2:0]	GNSS - input B signal	(Input)	—	—
INPUT_B1[2:0]	GNSS - input B signal	(Input)	—	—
INPUT_B2[2:0]	GNSS - input B signal	(Input)	—	—
INPUT_B3[2:0]	GNSS - input B signal	(Input)	—	—
DA_OUT[3:0]	GNSS - output signal	(Output)	—	—

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Signal Name	Function Definition	Direction	Active Level	Comments
UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)				
UART0_RX	UART0 - receiver signal	(Input)	—	—
UART0_TX	UART0- transmitter signal	(Output)	—	—
UART1_RX	UART1 - receiver signal	(Input)	—	—
UART1_TX	UART1- transmitter signal	(Output)	—	—
SERIAL PERIPHERAL INTERFACE (SPI)				
SPI_IN_CLK	SPI - clock input signal	(Input)	—	—
SPI_OUT_CLK	SPI - clock output signal	(Output)	—	—
SPI_SEL_N[4:0]	SPI - chip select signal	(Output)	Low	—
MOSI	SPI - Master Out - Slave In signal	(Output)	—	—
MISO	SPI - Master In - Slave Out signal	(Input)	—	—
EEPROM				
EEPROM_RESET_N	EEPROM reset signal	(Output)	Low	—
EEPROM_ENABLE	EEPROM enable signal	(Output)	High	—
EEPROM_POWER	EEPROM power pin	(Output)	High	—
DEBUG SUPPORT UNIT (DSU)				
DSU_ACT	DSU - active signal	(Output)	High	—
DSU_BRE	DSU - break	(Input)	rising edge	For final application, the pin shall be driven low.
DSU_EN	DSU - enable	(Input)	High	For final application, the pin shall be driven low.
DSU_SPW_EN	DSU - SpaceWire enable	(Input)	High	For final application, the pin shall be driven low.
DSU_SPW_TX_D	DSU - SpaceWire transmitter data signal	(Output)	—	—
DSU_SPW_TX_S	DSU - SpaceWire transmitter strobe signal	(Output)	—	—
DSU_SPW_RX_D	DSU - SpaceWire receiver data signal	(Input)	—	—
DSU_SPW_RX_S	DSU - SpaceWire receiver strobe signal	(Input)	—	—
DSU_UART_RX	DSU - UART receiver signal	(Input)	—	—
DSU_UART_TX	DSU - UART transmitter signal	(Output)	—	—
TEST MODE - OBSERVABILITY - INTERNAL USAGE				

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Signal Name	Function Definition	Direction	Active Level	Comments
SIGNAL_OUT_I[2:0]	Test mode - observability test signal out signal	(Output)	—	—
SIGNAL_OUT_Q[2:0]	Test mode - observability test signal out signal	(Output)	—	—
CODE_OUT2[1:0]	Test mode - observability GNSS - delay line signal	(Output)	—	—
CODE_OUT1[1:0]	Test mode - observability GNSS - delay line signal	(Output)	—	—
INT_EPOCH1	Test mode - observability GNSS - epoch integration signal	(Output)	—	—
INT_EPOCH2	Test mode - observability GNSS - epoch integration signal	(Output)	—	—
TEST_EN	Test mode enable pin signal	(Input)	High	For final application, the pin shall be driven low.
SCAN_EN	Test mode -scan test pin signal	(Input)	High	For final application, the pin shall be driven low.
SCAN_IN[11:0]	Test mode - scan input signal	(Input)	High	For final application, the pin shall be driven low.
TEST MODE - JTAG - INTERNAL USAGE				
TRST_N	JTAG interface test reset signal	(Input)	Low	External pull up shall be applied on this pin. Final application shall be driven low.
TCK	JTAG interface test clock signal	(Input)	—	External pull down shall be applied on this pin. For final application, the pin shall be driven low.
TDO	JTAG interface test data output signal	(Output)	—	—
TMS	JTAG interface test mode select signal	(Input)	—	For final application, the pin shall be driven low.
TDI	JTAG interface test data input signal	(Input)	—	For final application, the pin shall be driven low.
POWER				
PVDDBx	Power periphery power supply	(Input)	—	—
PVSSBx	Power periphery ground	(Input)	—	—
PVSSPLLx	Power PLL ground	(Input)	—	—

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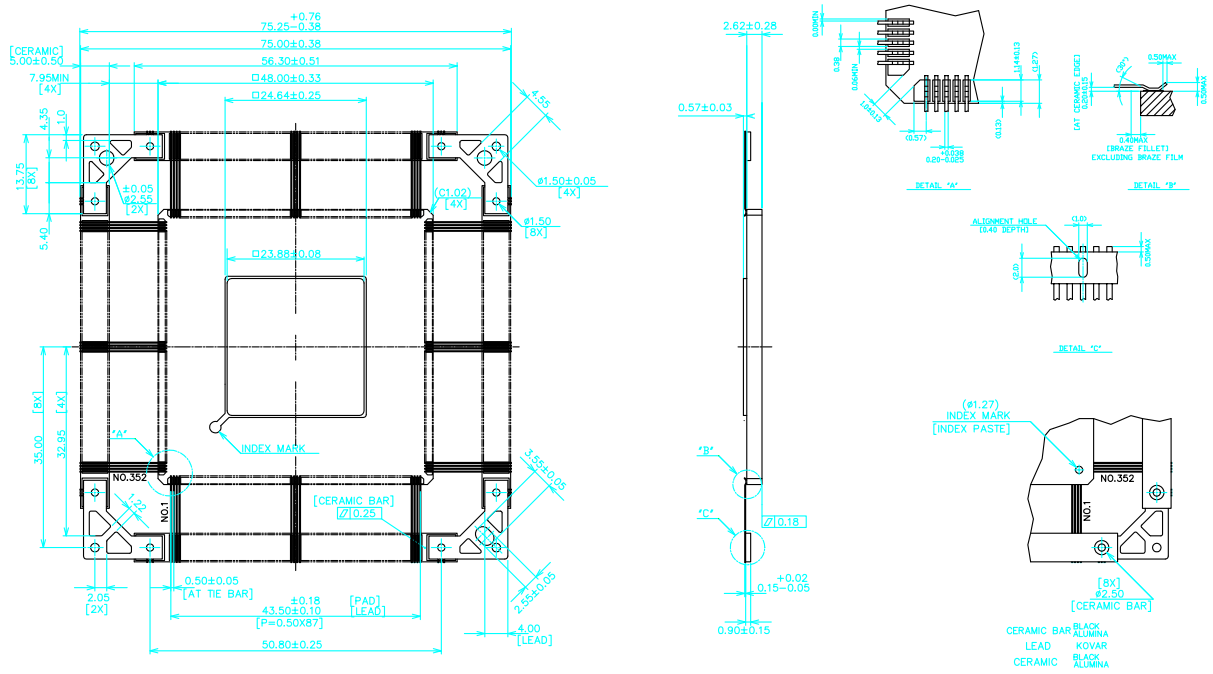
Signal Name	Function Definition	Direction	Active Level	Comments
PVDDPLLx	Power PLL power supply	(Input)	—	—
GND_ARRAY	Power core ground	(Input)	—	—
VCC_ARRAY	Power core power supply	(Input)	—	—

3. Package and Pinout

The following sections list the AT7991 package and pinout details.

3.1 Package Drawing

Figure 3-1. MQFP352 Package Drawing



3.2 MQFP352 Pinout

Table 3-1. MQFP352 Pinout (1/3)

Pin	Signal Name	Buffer	Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
1	NC		45	PVSSB3	pv33e00z	89	SYS_PLL_LOCK	pt33o01z
2	SYS_PLL_BYPASS	pc33d00z	46	GPIO[11]	pt33b01z	90	ADDRESS[7]	pt33o04z
3	RESERVED0	pc33d20z	47	SPW_RX_D[3]	pc33d00z	91	PVSSB7	pv33e00z
4	RESERVED0	pc33d20z	48	SPW_RX_S[3]	pc33d00z	92	PVDDB7	pv33ep33z
5	RESERVED0	pc33d00z	49	GPIO[12]	pt33b01z	93	ADDRESS[8]	pt33o04z
6	RESERVED0	pc33d00z	50	SPW_TX_D[3]	pt33o04z	94	ADDRESS[9]	pt33o04z
7	GND_ARRAY	pv33i00z	51	SPW_TX_S[3]	pt33o04z	95	GND_ARRAY	pv33i00z
8	VCC_ARRAY	pv33i18z	52	DSU_UART_RX	pc33d00z	96	VCC_ARRAY	pv33i18z
9	NC	pt33t01z	53	DSU_UART_TX	pt33o01z	97	ADDRESS[10]	pt33o04z
10	RESERVED0	pc33d00z	54	AGGA4_RESET_N	pc33d20z	98	ADDRESS[11]	pt33o04z

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Pin	Signal Name	Buffer	Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
11	RESERVED0	pc33d00z	55	PWR_ON_RESET_N	pc33d20z	99	ADDRESS[12]	pt33o04z
12	UART0_RX	pc33d00z	56	DSU_SPW_EN	pc33d20z	100	PVDDB8	pv33ep33z
13	UART0_TX	pt33o01z	57	ERROR_N	pt33t01z	101	PVSSB8	pv33e00z
14	UART1_RX	pc33d00z	58	NMI_INT	pc33d20z	102	ADDRESS[13]	pt33o04z
15	UART1_TX	pt33o01z	59	PVDDB4	pv33ep33z	103	ADDRESS[14]	pt33o04z
16	SPI_IN_CLK	pc33d00z	60	PVSSB4	pv33e00z	104	ADDRESS[15]	pt33o04z
17	SPI_OUT_CLK	pt33o01z	61	WDOG1_N	pt33t02z	105	ADDRESS[16]	pt33o04z
18	MOSI	pt33o01z	62	WDOG2_ N	pt33t02z	106	ADDRESS[17]	pt33o04z
19	MISO	pc33d00z	63	DSU_SPW_TX_D	pt33o04z	107	PVDDB9	pv33ep33z
20	SPI_SEL_N[0]	pt33o01z	64	DSU_SPW_TX_S	pt33o04z	108	PVSSB9	pv33e00z
21	SPI_SEL_N[1]	pt33o01z	65	EXT_SYS_CLK	pc33d00z	109	ADDRESS[18]	pt33o04z
22	SPI_SEL_N[2]	pt33o01z	66	DSU_SPW_RX_D	pc33d00z	110	ADDRESS[19]	pt33o04z
23	SPI_SEL_N[3]	pt33o01z	67	DSU_SPW_RX_S	pc33d00z	111	ADDRESS[20]	pt33o04z
24	PVDDB1	pv33ep33z	68	NC		112	ADDRESS[21]	pt33o04z
25	PVSSB1	pv33e00z	69	PVSSPLL1	pv18ft	113	ADDRESS[22]	pt33o04z
26	SPW_RX_D[0]	pc33d00z	70	PVDDPLL1	pv18ft	114	PVDDB10	pv33ep33z
27	SPW_RX_S[0]	pc33d00z	71	PVDDB5	pv33ep33z	115	PVSSB10	pv33e00z
28	GPIO[7]	pt33b01z	72	PVSSB5	pv33e00z	116	ADDRESS[23]	pt33o04z
29	SPW_TX_D[0]	pt33o04z	73	ADDRESS[0]	pt33o04z	117	ADDRESS[24]	pt33o04z
30	SPW_TX_S[0]	pt33o04z	74	ADDRESS[1]	pt33o04z	118	ADDRESS[25]	pt33o04z
31	GPIO[8]	pt33b01z	75	ADDRESS[2]	pt33o04z	119	ADDRESS[26]	pt33o04z
32	SPW_RX_D[1]	pc33d00z	76	ADDRESS[3]	pt33o04z	120	ADDRESS[27]	pt33o04z
33	SPW_RX_S[1]	pc33d00z	77	ADDRESS[4]	pt33o04z	121	PVDDB11	pv33ep33z
34	PVDDB2	pv33ep33z	78	ADDRESS[5]	pt33o04z	122	PVSSB11	pv33e00z
35	PVSSB2	pv33e00z	79	PVSSB6	pv33e00z	123	IOS_N	pt33o01z
36	SPW_TX_D[1]	pt33o04z	80	PVDDB6	pv33ep33z	124	RAMS_N[0]	pt33o04z
37	SPW_TX_S[1]	pt33o04z	81	GND_ARRAY	pv33i00z	125	RAMS_N[1]	pt33o04z
38	GPIO[9]	pt33b01z	82	VCC_ARRAY	pv33i18z	126	RAMS_N[2]	pt33o04z
39	SPW_RX_D[2]	pc33d00z	83	PVSSPLL2	pv18ft	127	RAMS_N[3]	pt33o04z
40	SPW_RX_S[2]	pc33d00z	84	PVDDPLL2	pv18ft	128	RAMS_N[4]	pt33o04z
41	GPIO[10]	pt33b01z	85	NC		129	PVDDB12	pv33ep33z
42	SPW_TX_D[2]	pt33o04z	86	ADDRESS[6]	pt33o04z	130	PVSSB12	pv33e00z
43	SPW_TX_S[2]	pt33o04z	87	MIL_PLL_LOCK	pt33o01z	131	ROMS_N[0]	pt33o01z
44	PVDDB3	pv33ep33z	88	EXT_MIL_CLK	pc33d00z	132	ROMS_N[1]	pt33o01z

Table 3-2. MQFP352 Pinout (2/3)

Pin	Signal Name	Buffer	Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
133	RAMOE_N[1]	pt33o04z	177	DATA[25]	pt33b04z	221	MIL_TX1B	pt33o01z
134	OE_N	pt33o01z	178	DATA[26]	pt33b04z	222	PVSSB23	pv33e00z
135	WRITE_N	pt33b04z	179	DATA[27]	pt33b04z	223	PVDDB23	pv33ep33z
136	RAMOE_N[0]	pt33o04z	180	DATA[28]	pt33b04z	224	MIL_TX1INH	pt33o01z
137	NC		181	DATA[29]	pt33b04z	225	RESERVED0	pc33d00z
138	PVDDB13	pv33ep33z	182	RESERVED0	pc33d00z	226	MIL_RESET_OUT_N	pt33t02z
139	PVSSB13	pv33e00z	183	GND_ARRAY	pv33i00z	227	SIGNAL_OUT_I[0]	pt33o01z
140	DATA[0]	pt33b04z	184	VCC_ARRAY	pv33i18z	228	SIGNAL_OUT_I[1]	pt33o01z
141	DATA[1]	pt33b04z	185	PVDDB19	pv33ep33z	229	SIGNAL_OUT_I[2]	pt33o01z
142	DATA[2]	pt33b04z	186	PVSSB19	pv33e00z	230	SIGNAL_OUT_Q[0]	pt33o01z
143	DATA[3]	pt33b04z	187	DATA[30]	pt33b04z	231	SIGNAL_OUT_Q[1]	pt33o01z
144	DATA[4]	pt33b04z	188	DATA[31]	pt33b04z	232	SIGNAL_OUT_Q[2]	pt33o01z
145	PVDDB14	pv33ep33z	189	CB[0]	pt33b04z	233	PVDDB24	pv33ep33z
146	PVSSB14	pv33e00z	190	CB[1]	pt33b04z	234	PVSSB24	pv33e00z
147	DATA[5]	pt33b04z	191	PVSSB20	pv33e00z	235	INT_EPOCH1	pt33o01z
148	DATA[6]	pt33b04z	192	CB[2]	pt33b04z	236	CODE_OUT2[0]	pt33o01z
149	DATA[7]	pt33b04z	193	PVDDB20	pv33ep33z	237	CODE_OUT2[1]	pt33o01z
150	DATA[8]	pt33b04z	194	CB[3]	pt33b04z	238	INT_EPOCH2	pt33o01z
151	DATA[9]	pt33b04z	195	CB[4]	pt33b04z	239	SPI_SEL_N[4]	pt33o01z
152	PVDDB15	pv33ep33z	196	CB[5]	pt33b04z	240	RESERVED0	pc33d00z
153	PVSSB15	pv33e00z	197	PVDDB21	pv33ep33z	241	RESERVED0	pc33d00z
154	DATA[10]	pt33b04z	198	PVSSB21	pv33e00z	242	CODE_OUT1[0]	pt33o01z
155	DATA[11]	pt33b04z	199	CB[6]	pt33b04z	243	CODE_OUT1[1]	pt33o01z
156	DATA[12]	pt33b04z	200	BEXC_N	pc33d00z	244	RESERVED0	pc33d00uz
157	DATA[13]	pt33b04z	201	BRDY_N	pc33d00z	245	RESERVED0	pc33d00uz
158	DATA[14]	pt33b04z	202	SGPO	pt33o01z	246	RESERVED0	pc33d00uz
159	PVDDB16	pv33ep33z	203	RWE_N[0]	pt33b04z	247	RESERVED1	pc33d00uz
160	PVSSB16	pv33e00z	204	RWE_N[1]	pt33b04z	248	PVDDB30	pv33ep33z
161	DATA[15]	pt33b04z	205	RWE_N[2]	pt33b04z	249	PVSSB30	pv33e00z
162	DATA[16]	pt33b04z	206	RWE_N[3]	pt33b04z	250	GPIO[13]	pt33b01z
163	DATA[17]	pt33b04z	207	READ	pt33o04z	251	GPIO[14]	pt33b01z
164	DATA[18]	pt33b04z	208	PVSSB22	pv33e00z	252	EEPROM_RESET_N	pt33o01z
165	DATA[19]	pt33b04z	209	PVDDB22	pv33ep33z	253	EEPROM_ENABLE	pt33o01z
166	PVDDB17	pv33ep33z	210	MIL_RX0	pc33d00z	254	SYS_PLL_FREQSEL	pc33d00dz
167	PVSSB17	pv33e00z	211	MIL_RX0B	pc33d00z	255	RESERVED0	pc33d00dz

.....continued

Pin	Signal Name	Buffer	Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
168	DATA[20]	pt33b04z	212	MIL_TX0	pt33o01z	256	GPIO[15]	pt33b01z
169	GND_ARRAY	pv33i00z	213	MIL_TX0B	pt33o01z	257	GND_ARRAY	pv33i00z
170	VCC_ARRAY	pv33i18z	214	DSU_ACT	pt33o01z	258	VCC_ARRAY	pv33i18z
171	DATA[21]	pt33b04z	215	DSU_BRE	pc33d00z	259	EEPROM_POWER	pt33o01z
172	DATA[22]	pt33b04z	216	DSU_EN	pc33d00z	260	RESERVED0	pc33d00z
173	DATA[23]	pt33b04z	217	MIL_TX0INH	pt33o01z	261	RESERVED0	pc33d00z
174	DATA[24]	pt33b04z	218	MIL_RX1	pc33d00z	262	RESERVED0	pc33d00z
175	PVSSB18	pv33e00z	219	MIL_RX1B	pc33d00z	263	RESERVED0	pc33d00z
176	PVDDB18	pv33ep33z	220	MIL_TX1	pt33o01z	264	RESERVED0	pc33d00z

Table 3-3. MQFP352 Pinout (3/3)

Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
265	EXT_CORE_CLK	pc33d00z	309	PIO[11]	pt33b01z
266	GNSS_RESET_N	pc33d20z	310	PIO[12]	pt33b01z
267	HALF_SAMPLE_CLK	pc33d00z	311	PIO[13]	pt33b01z
268	INPUT_A0[0]	pc33d00z	312	PIO[14]	pt33b01z
269	PVDDB25	pv33ep33z	313	PIO[15]	pt33b01z
270	PVSSB25	pv33e00z	314	GPIO[0]	pt33b01z
271	GND_ARRAY	pv33i00z	315	GPIO[1]	pt33b01z
272	VCC_ARRAY	pv33i18z	316	GPIO[2]	pt33b01z
273	INPUT_A0[1]	pc33d00z	317	GPIO[3]	pt33b01z
274	INPUT_A0[2]	pc33d00z	318	PVDDB27	pv33ep33z
275	INPUT_A1[0]	pc33d00z	319	PVSSB27	pv33e00z
276	INPUT_A1[1]	pc33d00z	320	GPIO[4]	pt33b01z
277	INPUT_A1[2]	pc33d00z	321	GPIO[5]	pt33b01z
278	INPUT_A2[0]	pc33d00z	322	GPIO[6]	pt33b01z
279	INPUT_A2[1]	pc33d00z	323	RESERVED0	pc33d00z
280	INPUT_A2[2]	pc33d00z	324	ASC[0]	pt33o01z
281	INPUT_A3[0]	pc33d00z	325	ASC[1]	pt33o01z
282	INPUT_A3[1]	pc33d00z	326	ASEO	pt33o01z
283	INPUT_A3[2]	pc33d00z	327	ASEI	pc33d20z
284	INPUT_B0[0]	pc33d00z	328	MEO	pt33o01z
285	INPUT_B0[1]	pc33d00z	329	MEI	pc33d20z
286	INPUT_B0[2]	pc33d00z	330	RESERVED0	pc33d00z
287	INPUT_B1[0]	pc33d00z	331	RESERVED0	pc33d00z

.....continued

Pin	Signal Name	Buffer	Pin	Signal Name	Buffer
288	INPUT_B1[1]	pc33d00z	332	PPSO	pt33o01z
289	INPUT_B1[2]	pc33d00z	333	PPSI	pc33d20z
290	INPUT_B2[0]	pc33d00z	334	EXT_CLK	pc33d00z
291	INPUT_B2[1]	pc33d00z	335	AU_TRIGGER	pc33d20z
292	INPUT_B2[2]	pc33d00z	336	SYS_CLK_OUT	pt33o01z
293	INPUT_B3[0]	pc33d00z	337	PVDDB28	pv33ep33z
294	PVDDB26	pv33ep33z	338	PVSSB28	pv33e00z
295	PVSSB26	pv33e00z	339	DA_OUT[0]	pt33o01z
296	INPUT_B3[1]	pc33d00z	340	DA_OUT[1]	pt33o01z
297	INPUT_B3[2]	pc33d00z	341	DA_OUT[2]	pt33o01z
298	PIO[0]	pt33b01z	342	DA_OUT[3]	pt33o01z
299	PIO[1]	pt33b01z	343	IMT_12	pt33o01z
300	PIO[2]	pt33b01z	344	SYS_CLK_DIV[0]	pc33d00uz
301	PIO[3]	pt33b01z	345	GND_ARRAY	pv33i00z
302	PIO[4]	pt33b01z	346	VCC_ARRAY	pv33i18z
303	PIO[5]	pt33b01z	347	SYS_CLK_DIV[1]	pc33d00uz
304	PIO[6]	pt33b01z	348	SYS_CLK_DIV[2]	pc33d00uz
305	PIO[7]	pt33b01z	349	SYS_CLK_DIV[3]	pc33d00uz
306	PIO[8]	pt33b01z	350	PVDDB29	pv33ep33z
307	PIO[9]	pt33b01z	351	PVSSB29	pv33e00z
308	PIO[10]	pt33b01z	352	MIL_CLK_OUT	pt33o01z

NC: Not Connected – Do not connect

RESERVED 0: Drive low for flight applications

RESERVED1: Drive high for flight applications

Capacitive load derating of these buffers is provided in the AC section.

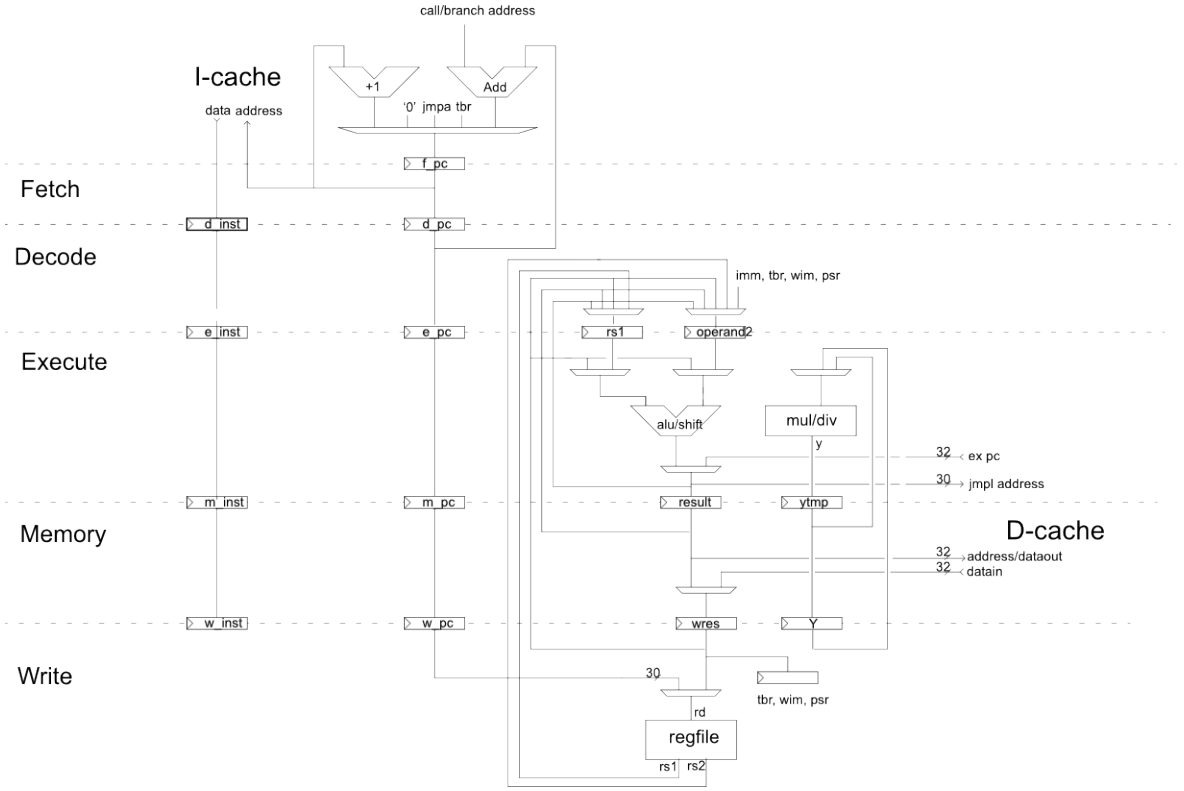
4. Product Description

4.1 Processor and Architecture

4.1.1 Integer Unit (IU)

The Leon2FT IU implements the SPARC integer instruction set as defined in the *SPARC Architecture Manual*.

Figure 4-1. Integer Unit Architecture



To execute instructions at a rate approaching one instruction per clock cycle, the IU employs a five-stage instruction pipeline that permits parallel execution of multiple instructions.

- Fetch: The instruction is fetched from the instruction cache is enabled and available or the fetch is forwarded to the memory controller.
- Decode: The instruction is placed in the instruction register and decoded. The operands are read from the register file and/or from immediate data and the next instruction computed CALL/Bicc target addresses are generated.
- Execute: Arithmetic, logical, and shift operations are performed and the result is saved in the temporary registers. Memory and JMPL/RETT target address are generated. Pending traps are prioritized and internal traps are taken, if any.
- Memory: On a memory load instruction, data is read from the data cache if enabled and available or the read is forwarded to the memory controller. On a memory store instruction, the stored data is always forwarded to the memory controller and any matching data cache entry is invalidated if enabled.
- Write: The result of any arithmetic, logical, shift, or memory/cache read operation is written back to the register file.

All the five stages operate in parallel, working on up to five different instructions at a time.

A basic “single-cycle” instruction enters the pipeline and completes in five cycles. By the time it reaches the write stage, four more instructions have entered and are moving through the pipeline behind it. Hence, after the first five cycles, a single-cycle instruction exits the pipeline and a single-cycle instruction enters the pipeline on every cycle.

4.1.1.1 Program Counters

The Program Counter (PC) contains the address of the instruction currently being executed by the Integer Unit, and the next Program Counter (nPC) holds the address (PC + 4) of the next instruction to be executed (assuming there is no control transfer and a trap does not occur). The nPC is necessary to implement delayed control transfers, wherein the instruction that immediately follows a control transfer may be executed before control is transferred to the target address.

Having both the PC and nPC available to the trap handler allows a trap handler to choose between retrying the instruction causing the trap (after the trap condition has been eliminated) or resuming program execution after the trap causing instruction.

4.1.1.2 Windowed Register File

The AT7991 processor contains a 136×32 register file divided into eight overlapping windows, each window providing a working registers set at a time. Working registers are used for normal operations and are called r registers.

The 136 registers are 32-bits wide and are divided into a set of eight global registers and a set of 128 window registers grouped into eight sets of 24 r registers called windows. At any given time, a program can access 32 active r registers (r0 to r31): eight (common) global registers (r0 to r7) and 24 window registers (r8 to r31) that are divided by software convention into eight ins, eight locals, and eight outs.

The first eight globals (r0 to r7) are also called g registers (g0 to g7), they usually hold common data to all functions (as a special case, r0/g0 always returns the value 0 when read and discards the value written to it)

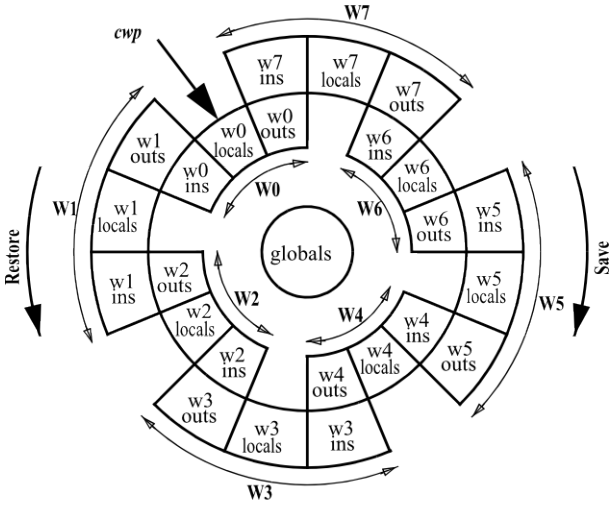
The next eight ins (r8 to r15) are also called i registers (i0 to i7), they usually are the input parameters of a function.

The next eight locals (r16 to r23) are also called l registers (l0 to l7); they usually are scratch registers that can be used for anything within a function.

The last eight outs (r24 to r31) are also called o registers (o0 to o7); they usually are the return parameters of a function.

The register file can be viewed as a circular stack, with the highest window joined to the lowest. Each window shares its INs and OUTs with the adjacent windows: OUTs from a previous window are the ins of the current window and the outs of the current window are the INs of the next window.

Figure 4-2. Circular Stack of Overlapping Windows



The register file implementation is based on two dual-port RAMs. The first dual-port RAM provides the first operand of a SPARC instruction while the second dual-port RAM provides the second operand unless an immediate value is needed. When applicable, the result of the instruction is written back into the register file, so the two dual-port RAMs always have equal contents.

When one function calls another, the calling function can choose to execute a SAVE instruction. This instruction decrements an internal counter, the Current Window Pointer (CWP), shifting the register window downward. The out registers of the caller then become the calling functions in registers and the calling function gets a new set of local and out registers for its own use. Only the pointer changes because the registers and the return address do not need to be stored on a stack. The RESTORE/RETT instructions acts in the opposite way

The Window Invalid Mask (WIM) register is controlled by supervisor software and is used by the hardware to determine whether a window overflow or underflow trap is to be generated by a SAVE, RESTORE, or RETT instruction.

When a SAVE, RESTORE, or RETT instruction is executed, the current value of the CWP is compared against the WIM register. If the SAVE, RESTORE, or RETT instruction would cause the CWP to point to an “invalid” register set, a window_overflow or window_underflow trap is caused.

4.1.1.3 Arithmetic and Logic Unit

The high-performance ALU operates in direct connection with all the 32 working registers. Within a single clock cycle, a 32-bit arithmetic operation between two working registers or between a working register and an immediate value is executed.

State Register

The Processor State Register (PSR) contains fields that report the status of the processor operations or control processor operations.

Instructions that modify its fields include SAVE, RESTORE, Ticc, RETT, and any instruction that modifies the condition code fields (icc). Any hardware or software action that generates a trap also modifies some of its fields.

A global interrupt management is provided: traps and interrupts (asynchronous traps) can be enabled/disabled and interrupts level response can be fine tuned.

Instruction Set

The AT7991 processor SPARC instructions fall into six functional categories: load/store, arithmetic/logical/ shift, control transfer, read/write control register, floating-point, and miscellaneous. Please refer to the SPARC V8 Architecture Manual for further details.

Multiply instructions

The AT7991 processor fully supports the SPARC V8 multiply instructions (UMUL, SMUL, UMULcc, and SMULcc). The multiply instructions perform a 32×32-bit integer multiply producing a 64-bit result. SMUL and SMULcc perform signed multiply while UMUL and UMULcc performs unsigned multiply. UMULcc and SMULcc also set the condition codes to reflect the result. The Y register holds the most-significant half of the 64-bit result.

Divide Instructions

The AT7991 processor fully supports the SPARC V8 divide instructions (UDIV, SDIV, UDIVcc, and SDIVcc). The divide instructions perform a 64×32 bit divide and produce a 32-bit result. SDIV and SDIVcc perform signed multiply while UDIV and UDIVcc performs unsigned divide. UDIVcc and SDIVcc also set the condition codes to reflect the result. Rounding and overflow detection is performed as defined in the SPARC V8 standard. The Y register holds the most-significant half of the 64-bit divided value.

4.1.2 Floating Point Unit (FPU)

The AT7991 uses the Gaisler Research Floating Point Unit (GRFPU). It is a high-performance FPU implementing floating-point operations as defined in IEEE Standard for Binary Floating-Point Arithmetic (IEEE-754) and SPARC V8 standard (IEEE-1754). Supported formats are single and double precision floating-point numbers. The advanced design combines two execution units, a fully pipelined unit for the execution of the most common FP operations and a non-blocking unit for the execution of the divide and square-root operations.

For more information, see *AT7991 User Manual*.

4.1.3 AMBA High Performances Bus (AHB)

The AT7991 processor uses standard AMBA AHB and APB internal buses.

For more information, see AMBA standard revision 2.

4.2 Clock and Reset Modules

4.2.1 Clock System

The clock system block is made up of:

- Two embedded PLLs with configurable or fixed ratio.
- Embedded dividers with fixed or configurable ratio.
- External input clocks (HALF_SAMPLE_CLK, EXT_CORE_CLK, EXT_MIL_CLK, EXT_SYS_CLK, SPI_IN_CLK).

It provides the following internal clocks:

- SysCLK is the system clock, (leon2core + periphery). This clock is also used for the MIL STD 1553B and the SpaceWire peripherals.
- SPICLK is the clock used for SPI interface.
- SpW 10 MHz Clk is used in the SpaceWire peripheral.
- 1553 clk is used in the MIL STD 1553B peripheral.
- halfSampleClk and CoreClock is used in the GNSS core.

It provides the following external clocks:

- SYS_CLK_OUT is a sense of SysCLK divided by 10.
- SPI_OUT_CLK is a sense of SPIclk.
- MIL_CLK_OUT is a sense of 1553clk divided by 4.

For more information, see AT7991 User Manual.

4.2.2 Reset

The AT7991 can be partially or globally reset depending on the reset source provided. The origin of the reset is stored in a dedicated register as well.

A global reset of the product can be launched by the PWR_ON_RESET_N pin.

A partial reset of the product (whole excluding the ResetStatusRegister) is achieved by the watchdog unit, by the AT7991_RESET_N pin or by software.

Some peripheral can be also reset independently:

- GNSS: by software or by GNSS_RESET_N pin
- SPW, MIL STD 1553B and /or UART: by software

For more information, see AT7991 User Manual.

4.3 Debug and Test Features

The AT7991 processor includes hardware debug support to aid software debugging on target hardware. The support is provided through two modules: a debug support unit (DSU) and a debug communication link (DCL). The DSU can put the processor in debug mode, allowing read/write access to all processor registers and cache memories. The DSU also contains a trace buffer which stores executed instructions or data transfers on the AMBA AHB bus. The debug communications link (UART or SpaceWire) implements a simple read/write protocol.

For more information, see AT7991 User Manual.

4.4 Traps and Interrupt Controllers

4.4.1 Traps

The AT7991 follows the general SPARC trap model.

For more information, see SPARC V8 Reference Manual and AT7991 User Manual.

4.4.2 Primary Interrupt Controller (PIC)

The PIC is used to prioritize and propagate requests from internal or external devices to Integer Unit (IU). 15 interrupts sources are handled with this PIC.

For more information, see AT7991 User Manual.

4.4.3 Communication Interrupt Controller (CIC)

An interrupt controller, dedicated to the communication interface is implemented inside the AT7991. Its outputs are directly connected to one PIC source, thus propagating interrupts to IU.

For more information, see AT7991 User Manual.

4.4.4 GNSS Interrupt Controller (GIC)

An interrupt controller, dedicated to the GNSS peripheral, is implemented inside the AT7991. The outputs are directly connected to two PIC sources, thus propagating interrupts to IU.

For more information, see AT7991 User Manual.

4.5 General Purpose Input/Output (GPIO)

32 GPIO are implemented inside the AT7991 product. Each GPIO line can be individually configured. They are divided into two separate controllers: 16 bit port I/O and GPIO.

4.5.1 16 Bit Port I/O (PIO)

16 bit PIO are accessible though this peripheral. Several peripherals are also muxed on this pins.

For more information, see AT7991 User Manual.

4.5.2 GPIO

16 additional GPIO are accessible though this peripheral.

For more information, see AT7991 User Manual.

4.5.3 S_GPO

A 16 bytes FIFO and a general purpose serial output pin (S_GPO) is available to transmit data flow.

4.6 External Memory Controller

The AT7991 embeds an external memory controller, aiming at supporting the following external devices: PROM, SRAM memories, and external devices connected to IO area.

The external memory controller embeds the following characteristics.

- ROM interface: eight or 32 bits, EDAC supported
- SRAM interface: eight or 32 bits, EDAC supported
- I/O interface: eight or 32 bits, EDAC supported
- Timing Parameters Specified by Software
- Write Protection for all RAM devices

For information on the functional behavior, see AT7991 User Manual.

4.7 Write Protection Unit

Write protection is provided to protect the RAM area against accidental over-writing. It is implemented with two methods.

- Address/mask method
- Start/end addressing method.

For information on the functional behavior, see *AT7991 User Manual*.

4.8 EEPROM Support Function

The AT7991 embed a functionality to power on/off by software an external EEPROM memory.

For information on the functional behavior, see *AT7991 User Manual*.

4.9 Fast Fourier Transform (FFT) Module

An FFT module is implemented inside the AT7991. It use the radix-2 algorithm and uses 128 points.

For information on the functional behavior, see AT7991 User Manual.

4.10 Cyclic Redundant Code (CRC) Module

A 32-bit CRC module is embedded inside the AT7991 product to increase data integrity.

For information on the functional behavior, see AT7991 User Manual.

4.11 Timers

AT7991 includes a general purpose Timer Unit that implements four 32-bit decrementing timers and one 10-bit shared prescaler.

For information on the functional behavior, see AT7991 User Manual.

4.12 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) circuit is a synchronous serial data link that provides communication with external devices in Master or Slave mode.

The SPI peripheral implemented inside the AT7991 has the following features.

- SPI master operation (clock master or clock slave)
- 8-bit to 16-bit programmable data length per chip select
- Programmable phase and polarity per chip select

For information on the functional behavior, see *AT7991 User Manual*.

4.13 Universal Asynchronous Receiver/Transmitter (UART)

Two identical DMA capable UARTs are provided for serial communications. The UARTs support data frames with 8 data bits, one optional parity bit and one stop bit. To generate the bit-rate, each UART has a programmable 12-bit clock divider. Hardware flow-control is supported through the RTSN/CTSN hand-shake signals.

For information on the functional behavior, see AT7991 User Manual.

4.14 SpaceWire (SpW)

The AT7991 provides a SpaceWire peripheral with 4 SpaceWire links, each data rate can reach 87 MHz. Dedicated DMA and interrupt capabilities are available for this peripheral.

For information on the functional behavior, see AT7991 User Manual.

4.15 MIL STD 1553B Link (1553)

The AT7991 embeds a MIL STD 1553B peripheral (Compliant to MIL-STD-1553B standard). Remote terminal configuration is supported on the AT7991. Secure link (data rate 1 Mbits/s) with a redundant interface is provided to secure spatial data.

For information on the functional behavior, see *AT7991 User Manual*.

4.16 Global Navigation Satellite System (GNSS)

The GNSS Core consists in four Input Modules (IM), one Power Level Detector (PLD) Module, two Beam Forming (DBF) Modules, a Time Base Generator (TBG), an Antenna Switch Controller (ASC), and 36 channels. Up to four RF front-end can be connected to the AT7991.

Every input module contains an Input Format Converter (IFC), two Digital Down Converter (DDCs), a Real to Complex Converter (R2C), and a D/A Converter in order to control an AGC in the RF Front-End. The Front End Interface is capable of processing wide-band signals up to 200 MHz and a variety of RF Front-End frequency plans.

Two Power Level Detector (PLD) modules are implemented: One PLD 5I, used for DDC module, and one PLD I/Q used in conjunction with the Input Format Converter (IFC) and the Final Down Converter (FDC)

The Digital Beam Forming (DBF) module combines the signals of two antenna elements in the digital domain in order to steer the antenna beam.

The Time Base Generator produces the Epoch Clock (EC), the Measurement Epoch (ME), and the Pulse-Per-Second (PPS).

The Antenna Switch Controller (ASC), consisting of the Antenna Switch Epoch Output (ASEO) Divider, a Synchroniser for the Antenna Switch Epoch Input (ASEI), and the Antenna Switch Sequencer.

36 channels are supported in the AT7991 product.

For information on the functional behavior, see *AT7991 User Manual*.

5. Fault Tolerant Features

To prevent erroneous operations due to the SEU/SET errors, the following hardening techniques are implemented in the AT7991 product.

- The main register file is implemented with hard flip flops.
- Most of the registers are using SEU hardened flip-flops, with exceptions in the GNSS datapath.
- Clocks, reset, and lock signals are implemented using TMR.
- An Error Detection And Correction (EDAC) is implemented to avoid single or multiple errors on external memories.
- The cache is protected using two parity bits.

6. Power Considerations

6.1 Power Supply

The following table defines the power supply rails of the AT7991.

Table 6-1. Power Supply Rails

Name	Voltage Nominal [V]	Voltage range [V]	Associated ground	Power
VCC_ARRAY	1.8	1.65 – 1.95	GND_ARRAY	core
PVDDBXX	3.3	3.0 – 3.6	PVSSBXX	periphery
PVDDPLL1	1.8	1.65 – 1.95	PVSSPLL1	PLL1
PVDDPLL2	1.8	1.65 – 1.95	PVSSPLL2	PLL2

6.2 Power Up/Down Sequences

6.2.1 Power Up

For power up, first power on PVDDBXX, and then power on VCC_ARRAY.

6.2.2 Power Down

For power down, first power off VCC_ARRAY, then power off PVDDBXX.

6.3 Power Consumption

Power consumption depends to a large extent on operating conditions, supply voltage, temperature, the activity of the chip (clock frequencies, number of channels activated), and output toggle rates. Based on simulation and measurement of selected scenarios, the following indicative values and formulae are provided.

- I/O power consumption at pins PVDDBx/PVSSBx: Beyond a static current of up to 2 mA, the dynamic consumption widely depends on the output toggle rate and load capacitance, it can be roughly calculated as:
  `Piodyn = ∑ (Ci * Vi2 + Pi )* Fi`

  Where,

  - Ci: the load capacitance of the output pins
  - Vi: the pin voltage of the output pins
  - Pi: the internal (dynamic) power of all the (input and output) pins, ~ 150 µW/MHz
  - Fi: the IO toggle frequency (rise + fall edge)
- Due to internal clock gating, the core power consumption largely depends on the number of channels activated (nChActive) in the ChActivation0|1 registers, an indicative value (in typical conditions) is given with the formula below:
  `Icore[mA] = (2.8 + 0.4 * nChActive) * CoreClk[MHz] + 9.2 * SysClk[MHz] + 10mA`

After reset (power-on or AGGA-4 reset), all channels are inactive, hence power consumption is reduced. But while reset is asserted, the clock gates are set to “active”, hence full power is consumed (nChActive = 36 in the above equation). The user should therefore limit the time at which device is at reset mode.

The board power supply must therefore make sure that the full current can be provided, even though the receiver might never activate all the channels. As the reset period is short, a possible alternative could be a capacitor, which is able to provide the necessary current for the time of reset. The longest possible reset duration (caused by the AT7991 chip itself) is 2209 EXT_SYS_CLK cycles + 4 CoreClk cycles.

Example:

- Assuming 200 IOs toggling at 10 MHz, of which 100 are outputs with load 50 pF, voltage 3.6 V, we get:
  `Piodyn = [100 * 50 * 13 + 200 * 150] * 10 µW = 0.95 W`
- Assuming the AT7991 is clocked with 80 MHz SysClk and 40 MHz GNSS CoreClk, then the maximum current on the 2 V core supply (for example, during reset) would be:
  `Icore = [ (2.8 + 0.4 * 36) * 40 + 9.2 * 80 + 10 ] mA = 1.5 A`

  Hence, the power consumption is ~ 3 W.

Table 6-2. Typical Power Consumption

Area	Power Consumption [mA/MHz]
Periphery	50 mA/MHz
Core	25 mA/MHz
GNSS	25 mA/MHz

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Storage Temperature……..-65°C to 150°C Operating Temperature ……..-55 °C to 125°C Maximum junction temperature (TJ) ..... 175°C Thermal resistance junction to case (Rjc) .....1°C/W Input Voltage on I/O Pins with Respect to Ground…… 0V to pvddbX Voltage on core (1.8V)…… -0.3 to 2V Voltage on I/O (3.3V)…… -0.3 to 4V DC current per I/O pins……..-10 mA to 10 mA ESD Performances……..1000 V, class 1 according to MIL-STD-883 as required in MIL-PRF-38535F	*Notice: Stresses beyond those listed under Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 DC Characteristics

Table 7-1. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vcc_array	DC supply core	—	1.65	1.8	1.95	V
pvddpll	DC supply PLL	—	1.65	1.8	1.95	V
pvddbX	DC supply array – standard IO	—	3.0	3.3	3.6	V
Vil	Low level Input voltage	—	-0.3	—	0.8	V
Vih	High level Input voltage	—	2	—	pvssbX +0.3	V
Vol	Low level Output voltage	IOL=2,4, 8,12,16mA	—	—	0.4	V
Voh	High level Output voltage	IOH=2,4, 8,12,16mA	pvddbX – 0.4	—		V
Vcsth	Cold sparing supply voltage threshold for CMOS	IICS < 4 µA		—	0.5	V
ICCSb	Standby current	—	—	—	34 mA	mA
IICS	Cold sparing leakage input current	pvddbX =Vss=0V Vin=0 to pvddbX	-1	—	1	µA
IOCS	Cold sparing leakage output current	pvddbX =Vss=0V Vout=0 to pvddbX	-1	—	1	µA
IIH	High level input current	Vin= pvddbX	-1	—	1	µA
	Pull up resistor		-5	—	5	µA
	Pull down resistor		140	320	600	µA

.....continued						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
IIL	low level input current	Vin=Vss	-1		1	µA
	Pull up resistor		110	220	400	µA
	Pull down resistor		-5		5	µA
IOZ	High impedance state output current	Vin= pvddbX or Vss No pull resistor	-1	—	1	µA

7.3 Cold Sparing

The cold sparing capability of the IOs allows to be electrically connected to a bus while its power supply remains in the range [PVSSBXX-300mV/ PVSSBXX +300mV], this without any risk of damage for the device. Cold-sparing allows a redundant spare to be electrically connected but unpowered until needed.

For applications requiring high reliability, the capability to use of a redundant device is a key feature. The cold sparing availability on the AGGA4 makes the product especially suitable for high reliability systems.

All the pads are cold sparing.

7.4 Decoupling Capacitance

There are three main frequencies involved in the processor: 40 MHz and 100 MHz for the GNSS interface, up to 87 MHz for the processor clock.

The following hypothesis is taken for the calculation of the decoupling capacitance.

- 1.5 nH is issued from the connection of the capacitor to the PCB
- 1.5 nH is issued from the capacitor intrinsic inductance

This hypothesis corresponds to a capacitor connected to two micro-vias on a PCB.

The filter defined by the inductance and the decoupling capacitor shall be able to filter the characteristic frequencies of the application. Each frequency to filter is defined by:

$$fc = \frac{1}{2\pi\sqrt{LC}}$$

Where,

- L: the inductance equivalent to the global inductance on the VSS18/VDD18 and VSS33/VCC33 lines.
- C: the decoupling capacitance.

For a processor running at 87 MHz with a GNSS interface at a characteristic frequency of 100 MHz and 40 MHz and considering that power supply pins are grouped by multiple of four, the decoupling capacitance to set are:

- 22 nF for 40 MHz decoupling
- 3 nF for 100 MHz decoupling

7.5 Pin Capacitance

Table 7-2. Capacitance Values

Parameter	Description	Max value
CIN	Standard input capacitance	7 pF
CIO	Standard input/output capacitance	7 pF

7.6 Clocks Characteristics

7.6.1 System Clock

The SysClk can be provided either directly by an external clock (ext_sys_clk) up to a frequency of 87 MHz or through the on-chip PLL up to a frequency of 80 MHz. When using the on-chip PLL, the frequency of the external clock (ext_sys_clk) shall be in the range [10-160 MHz] and then adjusted with an internal divider to match the internal constraint of 80 MHz.

Table 7-3. Input System Clocks Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ext_sys_clk (without system pll)	External system clock	—	—	—	87	MHz
Ext_sys_clk (with system pll)	External system clock	—	10	—	160	MHz
fin	Pll Input Frequency	—	—	10		MHz
fout	Pll Output Frequency	—	40	—	80	MHz
Ipll	Pll Current Consumption	—	—	—	9	mA
ts	Pll startup time	—	—	—	1	µs

Table 7-4. Supply Voltage Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
vddpllx	Supply voltage range	—	1.65	1.8	1.95	V

7.6.2 1553 Clock

The 16 MHz 1553clk clock can be provided either directly from the external clock (ext_mil_clk) or through an embedded dedicated PLL. In the two cases, the internal 1553clk clock shall be equal to 16 MHz to be aligned with the MIL-STD1553 constraints.

Table 7-5. Input 1553 Clocks Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ext_mil_clk	External 1553 clock	-	-	16	-	MHz
fin	Pll Input Frequency	-		10		MHz
fout	Pll Output Frequency	-		160		MHz
Ipll	Pll Current Consumption	-			9	mA
ts	Pll startup time				1.2	µs

Table 7-6. Supply Voltage Phase Lock Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
vddpllx	Supply voltage range	-	1.65	1.8	1.95	V

7.6.3 GNSS Clock

Two internal clocks (halfsampleclk and coreclk) are needed for the GNSS usage:

- halfsampleclk clock is directly feed by an external clock half_sample_clk
- coreclk can be directly feed by an external clock ext_core_clk or by halfsampleclk clock internally divided by a ratio of 2.5.

The maximum frequency allowable for half_sample_clk is 100 MHz. This induces a maximum halfsampleclk frequency of 100 MHz in return.

The maximum frequency allowable for coreclk is 40 MHz. Therefore, the maximum ext_core_clk frequency is 40 MHz.

Table 7-7. Input GNSS Clocks Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ext_core_clk	External GNSS CoreClock input	—	—	—	50	MHz
Half_sample_clk	External GNSS halfsample clock core input	—	—	—	100	MHz

7.6.4 SpaceWire Clock

Two internal clocks are necessary to use SpaceWire peripheral. The SpW 10 MHz clk and the Sysclk.

The SpW 10 MHz clk is fixed to 10 MHz and the sysclk is the system clock. The SpW 10 MHz clk is directly connected to the system pll input. Therefore, the sysclk feeds ext_sys_clk, passing through the system pll.

The resulting constraints for ext_sys_clk frequency range is 10 MHz–160 MHz in returns.

Table 7-8. SpaceWire Clocks Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ext_sys_clk (with system pll)	External system clock	—	10	—	160	MHz

7.6.5 SPI Clock

Two internal clocks can feed the SPIclk clock: an external one SPI_IN_CLK or the system clock sysclk divided by eight and a divider.

Table 7-9. Input SPI Clocks Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Spi_in_clk	Spi slave input clock	—	—	—	5	MHz

7.7 AC Characteristics

7.7.1 Test Conditions

Temperature range [-55°C – 125°C]

Voltage range:

- `Vcc_array=1.8V +/- 0.15`
- `pVddbX=3.3 +/- 0.3`

Voltage threshold Test condition pVddbX/2

The timing in the following sections has been calculated with the following nominal load in the output ports:

Table 7-10. Assumed Load for Timing Values

Port	Load (pF)
ADDRESS	30
DATA	50
CB	50

.....continued	
Port	**Load (pF)**
RAMS_N	20
ROMS_N	10
OE_N	25
WRITE_N	25
RAMOE_N	20
other signals	50

The delay of the output buffers can be derated depending on the actual load connected to the output port with the values given in Table 7.11. The derating is given as:

```
T = T0 + D*(CL-CN)
```

Where,

- T is resulting timing in ns
- T0 the nominal delay
- D the derating factor
- CL the actual and CN the nominal output load in pF.

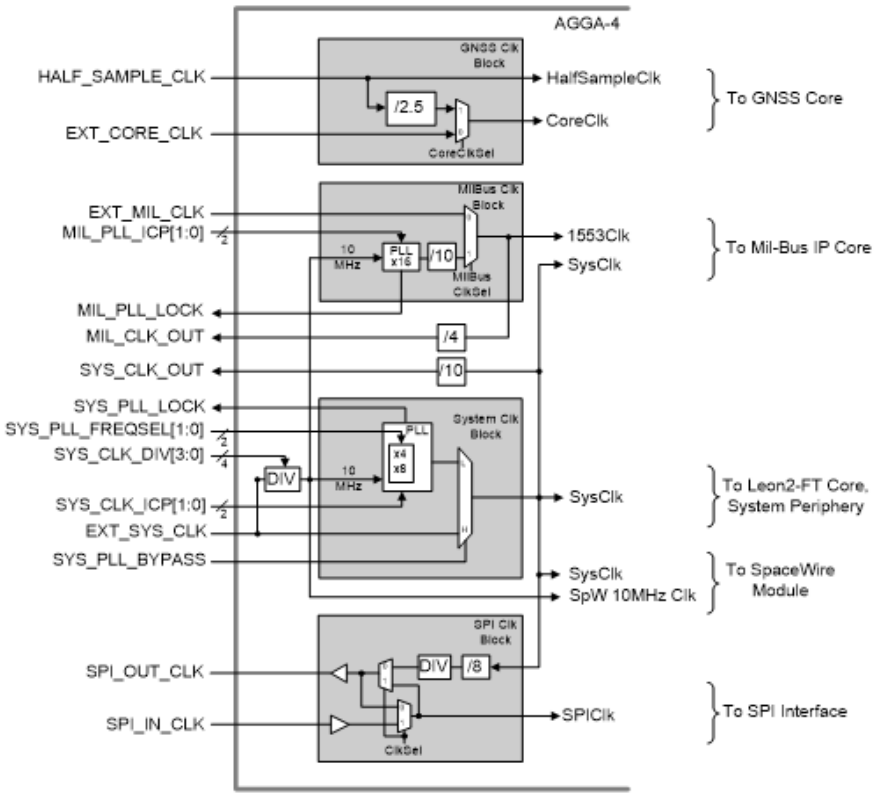
Table 7-11. Buffer Delay Derating (ns/pF)

Buffer Type	pt33o01z pt33t01z pt33t01dz pt33t01uz pt33b01z pt33b01dz pt33b01uz	pt33o02z pt33t02z pt33t02dz pt33t02uz pt33b02z pt33b02dz pt33b02uz	pt33o04z pt33t04z pt33t04dz pt33t04uz pt33b04z pt33b04dz pt33b04uz
Worst Case	0.21	0.11	0.058
Best Case	0.08	0.04	0.021

7.7.2 System Timings

The following figures presents the clock generation and distribution of the product. The minimum periods for the clock domains shown at the right side of the figure as well as other clocking constraints and recommendations. These minimum periods have to be respected from cycle-to-cycle, the jitter of the clock sources and the internal PLLs have to be considered, possibly leading to a reduced maximum frequency.

For details on the clock distribution, see AT7991 User Manual.



7.7.2.1 System Clock

Figure 7-1. System Clock with PLL Bypass

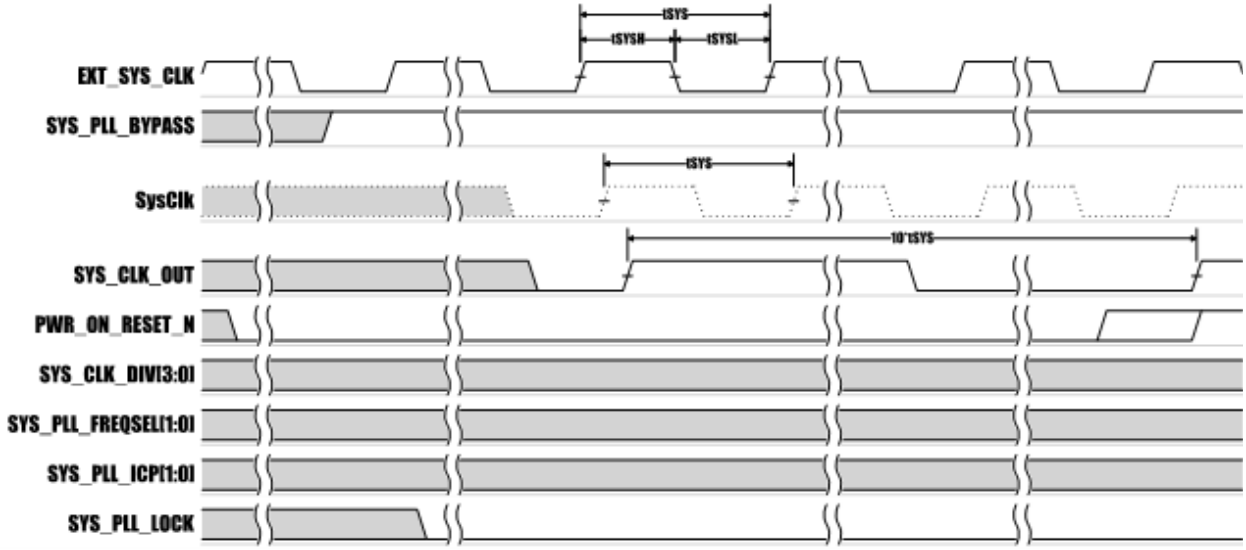


Figure 7-2. System Clock with PLL Active

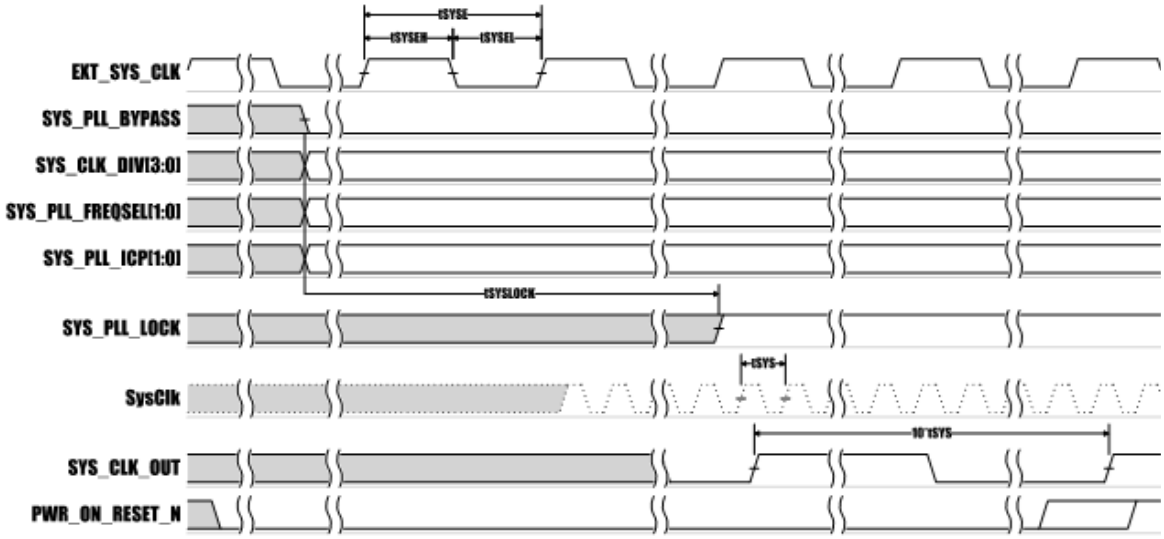


Table 7-12. System Clock Timings

Symbol	Description	Min (ns)	Max (ns)
tSYS	System clock period	11.5	25
tSYSH	System clock high duration (PLL off)	Refer to Table 7-3	
tSYSL	System clock low duration (PLL off)	Refer to Table 7-3	
tSYSE / DIV(1)	External system clock period (PLL on)	12.5	100
tSYSEH / DIV(1)	External system clock high duration (PLL on)	Refer to Table 7-37.3	
tSYSEL / DIV(1)	External system clock low duration (PLL on)	Refer toTable 7-3	
tSYSLOCK	System PLL startup time to lock	—	7 µs

Note:
DIV is the division factor represented by SYS_CLK_DIV[3:0] (1 ≤ DIV ≤ 16)

7.7.2.2 Reset Timing

Figure 7-3. Reset Timing

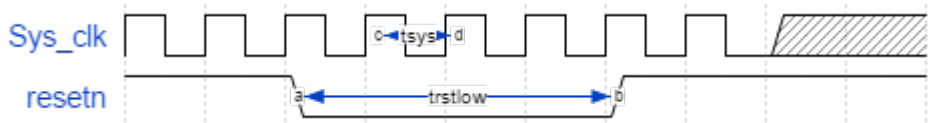


Table 7-13. Reset Timing

Symbol	Description	Conditions	Min	Typ	Max	Unit
tPOWER_RST_LOW	Reset low timing pulse duration (pin PWR_ON_RESET_N)	—	20	—	—	tsys
tAT7991_RST_LOW	Reset low timing pulse duration (pin AT7991_RESET_N)	—	20	—	—	tsys

.....continued

Symbol	Description	Conditions	Min	Typ	Max	Unit
tGNSS_RST_LOW	Reset low timing pulse duration (pin GNSS_RESET_N)	—	20	—	—	tsys

7.7.3 SRAM/PROM/IO Timing

Unless otherwise specified, adhere to the following table listing the reference load on the memory interface used for timing specification.

Table 7-14. Reference Load on Memory Interface

Port	Load (pF)
ADDRESS	30
DATA	50
CB	50
RAMS_N	20
ROMS_N	10
OE_N	25
WRITE_N	25
RAMOE_N	20
other pins	50

7.7.3.1 SRAM Memory

Figure 7-4. Fetch, Read and Write from 32-bit SRAM - n Waitstates , I/D caches Off

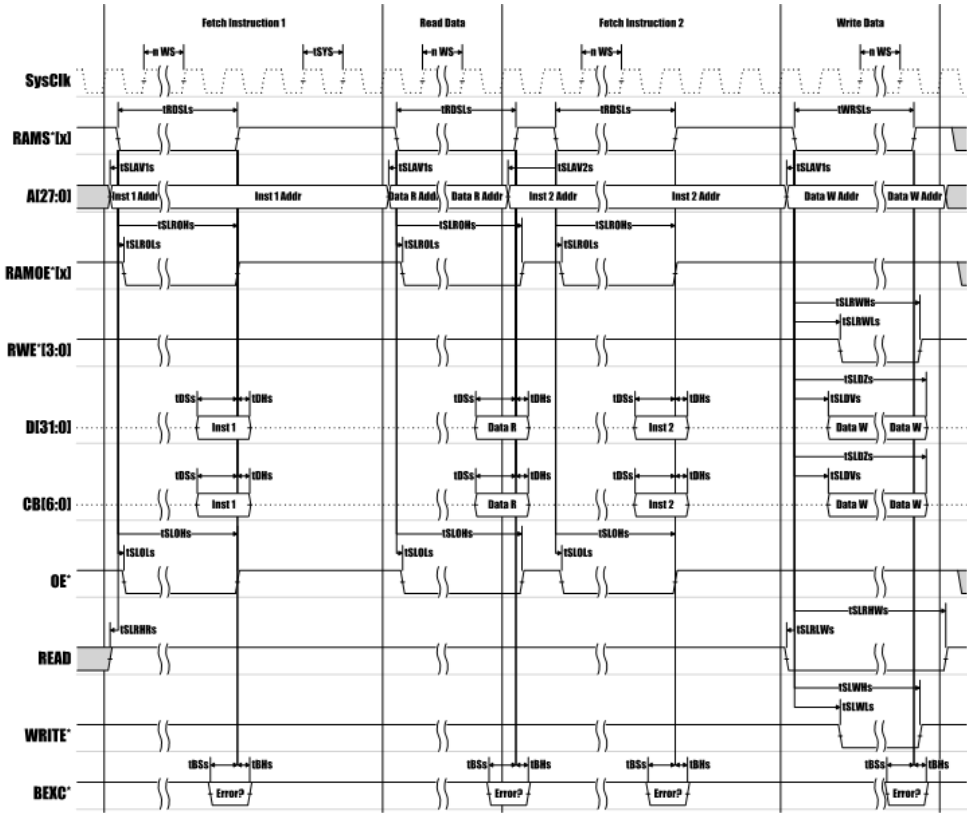


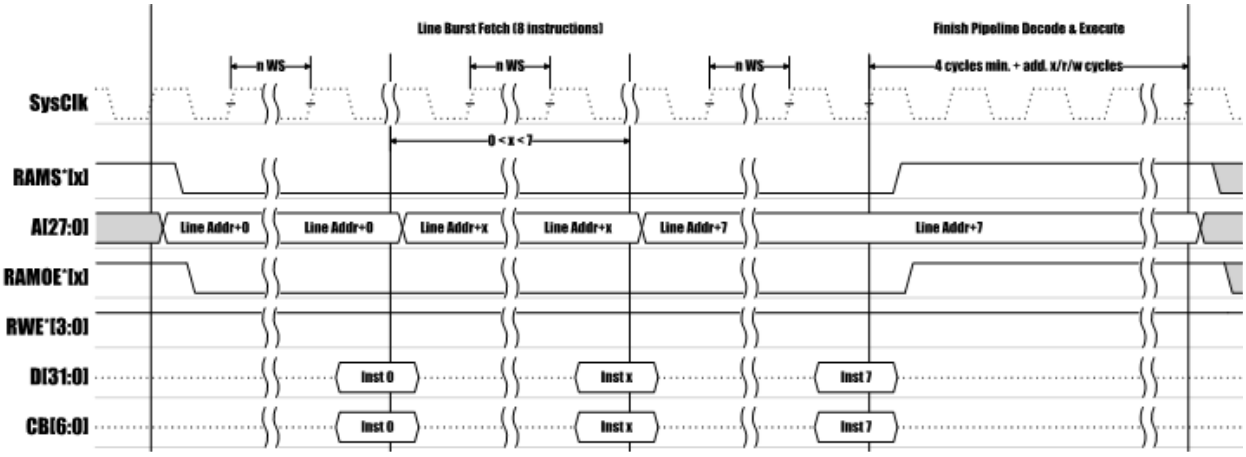
Table 7-15. SRAM Timings

Symbol	Description	Min (ns)	Max (ns)
t_{RDSLs}	SRAM chip select low duration (read)	(2+n) * tSYS	(2+n) * tSYS
t_{SLAV1s}	Address valid before SRAM chip select low 1	-1.3	-0.23
t_{SLAV2s}	Address valid before SRAM chip select low 2	-1.3 + tSYS	-0.23 + tSYS
t_{SLROLs}	SRAM output enable low after chip select low	0.4	0.5
t_{SLROHs}	SRAM output enable high after chip select low	0.4 + (2+n)*tSYS	0.5 + (2+n)*tSYS
t_{SLOLs}	Output enable low after chip select low	1.34	3.37
t_{SLOHs}	Output enable high after chip select low	1.34 + (2+n)*tSYS	3.37 + (2+n)*tSYS
t_{DSs}	Data setup time (read)	0.69	14.3
t_{DHs}	Data hold time (read)	-8.82	-3.74
t_{SLRHRs}	READ high before SRAM chip select low	1.02	2.85
t_{WRSLs}	SRAM chip select low duration during write	(2+n) * tSYS	(2+n) * tSYS
t_{SLRWLs}	SRAM write enable low after chip select low	-2.72 + tSYS	-1.02 + tSYS
t_{SLRWHs}	SRAM write enable high after chip select low	-2.72 + (2+n)*tSYS	-1.02 + (2+n)*tSYS

.....continued

Symbol	Description	Min (ns)	Max (ns)
t_{SLDVs}	Data valid after SRAM chip select low (write)	0.19 + tSYS	2.04 + tSYS
t_{SLRLWs}	READ low before SRAM chip select low	1.02	2.85
t_{SLRHWs}	READ high after SRAM chip select low	-2.72 + (3+n)*tSYS	-1.02 + (3 + n)*tSYS
t_{SLWLs}	WRITE low before SRAM chip select low	0.33 + tSYS	0.16 + tSYS
t_{SLWHs}	WRITE high after SRAM chip select low	0.33 + (2+n)*tSYS	0.16 + (2+n)*tSYS
t_{BSs}	BEXC setup time	-0.34	14.64
t_{BHs}	BECX hold time	-8.9	-3.28

Figure 7-5. Cache Line Burst Fetch from 32-bit SRAM - n Waitstates



7.7.3.2 PROM Memory

Figure 7-6. Fetch, Read and Write from 32-bit PROM - 2n wait-states, I/D Caches Off

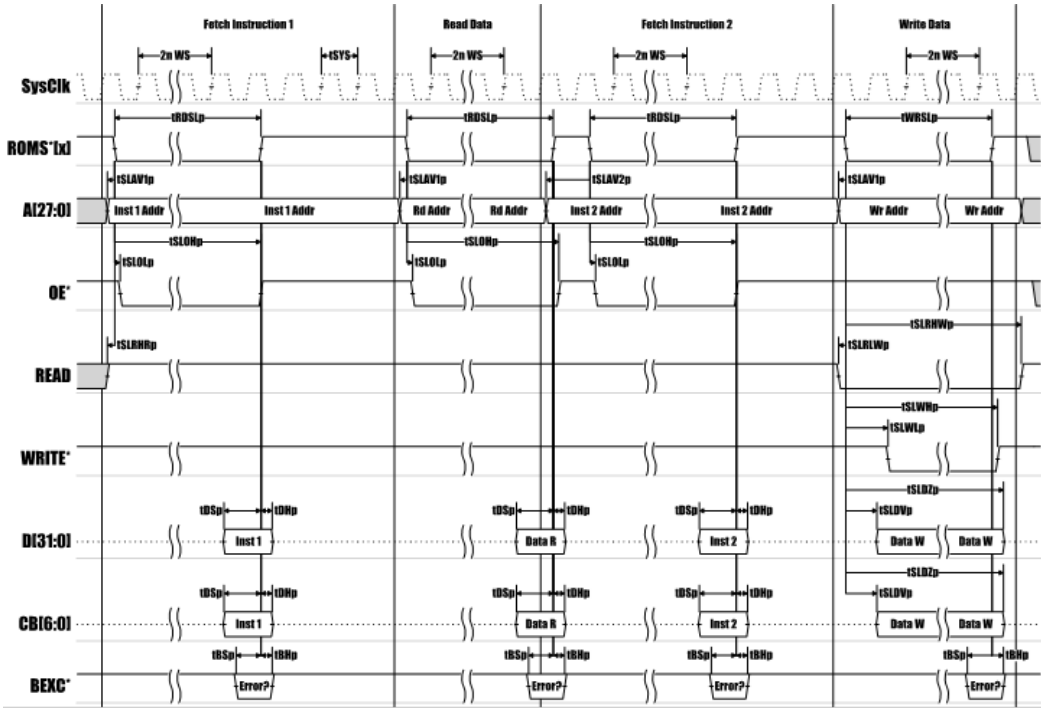


Table 7-16. PROM Timings

Symbol	Description	Min(ns)	Max(ns)
t_{RDSLp}	PROM chip select low duration (read)	(2+2n) * tSYS	(2+2n) * tSYS
t_{SLAV1p}	Address valid before PROM chip select low 1	0.06	0.59
t_{SLAV2p}	Address valid before PROM chip select low 2	0.06 + tSYS	0.59 + tSYS
t_{SLRHRp}	READ high before PROM chip select low	1.31	4.75
t_{SLOLp}	Output enable low after chip select low	1.05	1.47
t_{SLOHp}	Output enable high after chip select low	1.05 + (2 + 2n)*tSYS	1.47 + (2 + 2n)*tSYS
t_{DSp}	Data setup time (read)	1.03	16.2
t_{vDHp}	Data hold time (read)	-10.72	-4.03
t_{WRSLp}	PROM chip select low duration during write	(2+2n) * tSYS	(2+2n) * tSYS
t_{SLRLWp}	READ low before PROM chip select low	1.31	4.75
t_{SLRHWp}	READ high after PROM chip select low	-4.75+ (2n+3)*tSYS	-1.31+ (2n+3)*tSYS
t_{SLWLp}	WRITE low before PROM chip select low	-1.76 + tSYS	0.04 + tSYS
t_{SLWHp}	WRITE high after PROM chip select low	-1.76 + (2 + 2n)*tSYS	0.04 + (2 + 2n)*tSYS
t_{SLDVp}	Data valid after PROM chip select low (write)	-0.1 + tSYS	0.14 + tSYS
t_{BSp}	BEXC setup time	-0.05	16.54

7.7.3.3 IO Memory

Figure 7-7. Fetch (PROM), Read, Fetch (PROM) and Write from 32-bit IO - n Waitstates, I/D Caches Off

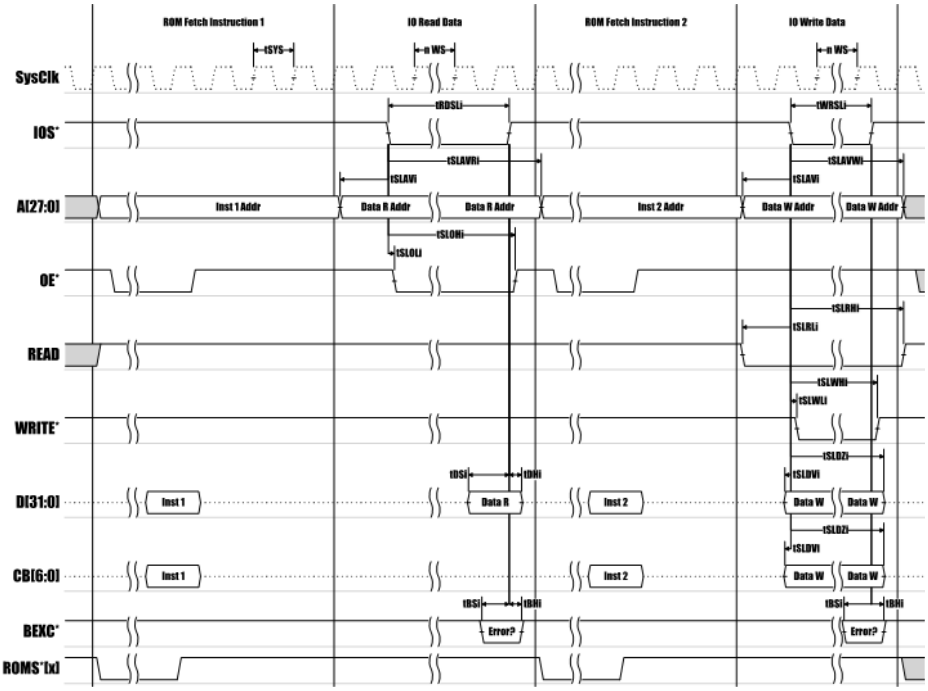
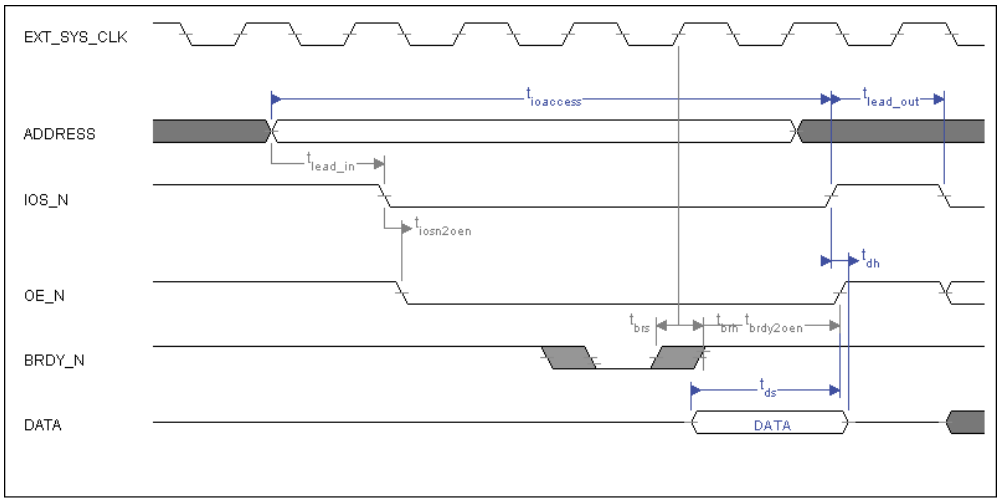


Table 7-17. IO Timings

Symbol	Description	Min(ns)	Max(ns)
tRDSLi	IO chip select low duration (read)	(2+n) * tSYS	(2+n) * tSYS
tSLAVi	Address valid before IO chip select low	-2.56 + tSYS	-0.53 + tSYS
tSLAVRi	Address valid after IO chip select low (read)	0.53 + (3+n)*tSYS	2.56+ (3+n)*tSYS
tSLOLi	Output enable low after IO chip select low	1.64	4.62
tDSi	Data setup time (read)	0.39	13.05
tDHi	Data hold time (read)	-7.57	-3.44
tWRSLi	IO chip select low duration (write)	(1+n) * tSYS	(1+n) * tSYS
tSLAVWi	Address valid after IO chip select low (write)	0.53 + (2+n)*tSYS	2.56+ (2+n)*tSYS
tSLRLi	READ low before IO chip select low during write	0.72 + tSYS	1.6 + tSYS
tSLRHi	READ high after IO chip select low during write	-1.6 + (2+n)*tSYS	-0.72 + (2+n)*tSYS
tSLWLi	WRITE* low before IO chip select low	0.63	1.39
tSLWHi	WRITE* high after IO chip select low	0.63 + (1+n)*tSYS	1.39 + (1+n)*tSYS
tSLDVi	Data valid after PROM chip select low (write)	-3.29	-0.49
tBSi	BEXC setup time	-0.64	13.39
tBHi	BECX hold time	-7.65	-2.98

7.7.3.4 BRDY_N usage

Figure 7-8. BRDY_N and BEXC_N_timing (Synchronous)



BRDY_N_and_BEXC_N_timing_(asynchronous)

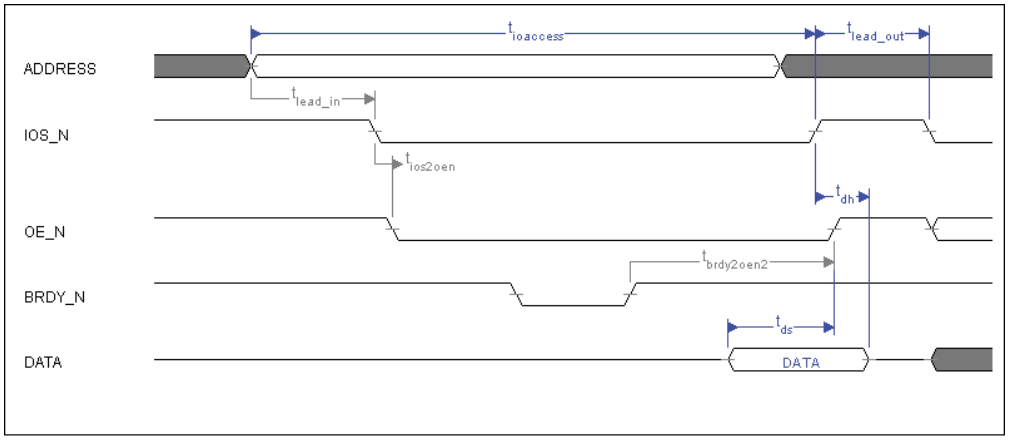


Table 7-18. BRDY_N and BEXC_N Timing

Symbol	Description	Min(ns)	Max(ns)
tBRS	Setup time of BRDY_N signal	-6.58	-2.44
tBRH	Hold time of BRDY_N signal	2.94	8.13

7.7.4 SpaceWire Timing

Figure 7-9. SpaceWire Timing Diagram

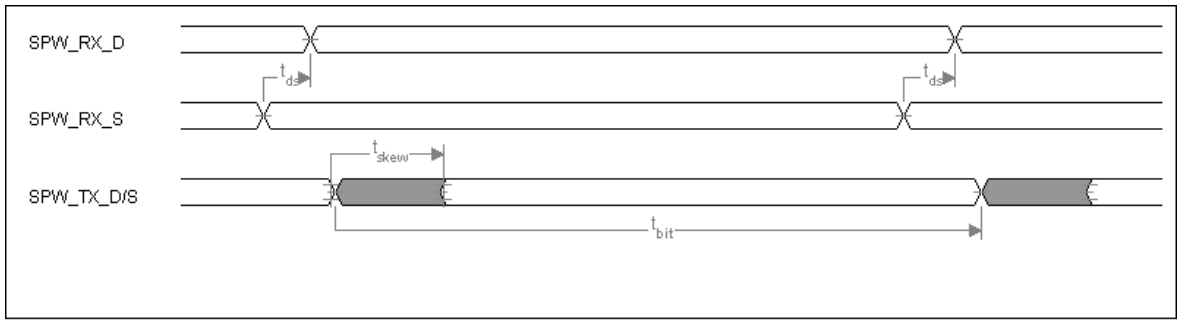


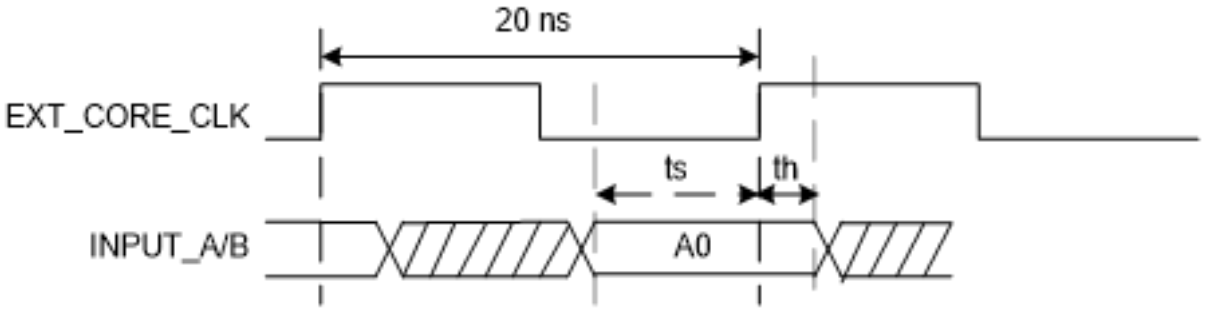
Table 7-19. SpaceWire Timing

Symbol	Description	Min(ns)	Max(ns)
tDS_TX	TX Data_Strobe_Skew	0	0.7
tDS_RX	RX Data_Strobe_Separation	—	1.5
tBIT	spw_bit_period	—	11.11

7.7.5 GNSS Timing

7.7.5.1 IFC Mode

Figure 7-10. GNSS IFC Mode



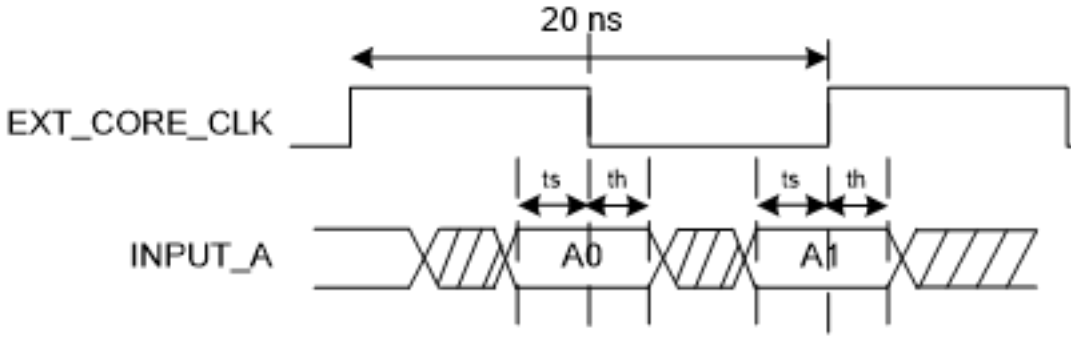
The following timings are given for the IFC mode worst case situation (EXT_CORE_CLK = 50 MHz).

Table 7-20. GNSS Timing parameters – IFC Mode

Symbol	Description	Min(ns)	Max(ns)
tIFC_S	IFC mode -Set up time	-1.7	—
tFC_H	IFC mode -Hold time	9.4	—

7.7.5.2 R2C Mode

Figure 7-11. GNSS R2C Mode



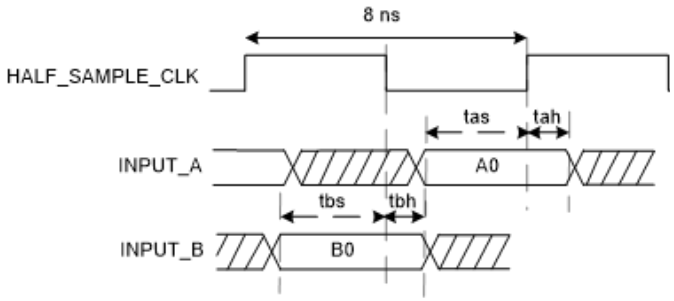
The following timings are given for the R2C mode worst case situation (EXT_CORE_CLK = 50 MHz).

Table 7-21. GNSS Timing Parameters – R2C Mode

Symbol	Description	Min(ns)	Max(ns)
tR2C_S	R2C mode -Set up time	2	-
tR2C_H	R2C mode -Hold time	3	-

7.7.5.3 DDC Mode

Figure 7-12. GNSS DDC Mode



The following timings are given for the DDC mode timing worst case situation (HALF_SAMPLE_CLK = 125 MHz)

Table 7-22. GNSS Timing parameters – DDC mode

Symbol	Description	Min(ns)	Max(ns)
tDDC_AS	DDC mode -Set up time	—	1.5
tDDC_AH	DDC mode - Hold time	—	3.3
tDDC_BS	DDC mode -Set up time	—	1.5
tDDC_BH	DDC mode - Hold time	—	3.3

7.7.6 SPI Timing

7.7.6.1 External SPI Clock

Figure 7-13. ClkSel = 1; RcvClkPol = 0; ClkPhase = 0; ClkPol = 0

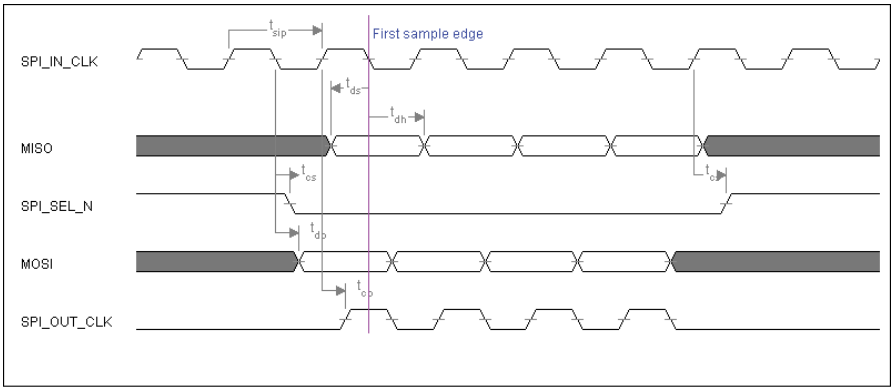


Figure 7-14. ClkSel = 1; RcvClkPol = 0; ClkPhase = 0; ClkPol = 1

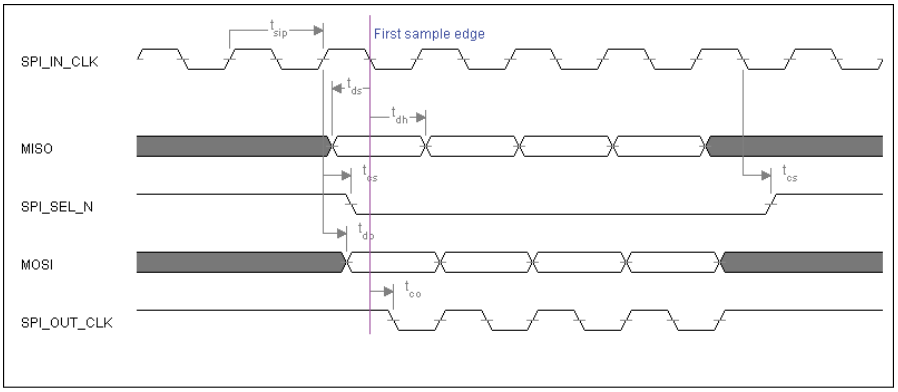


Figure 7-15. ClkSel = 1; RcvClkPol = 0; ClkPhase = 1; ClkPol = 0

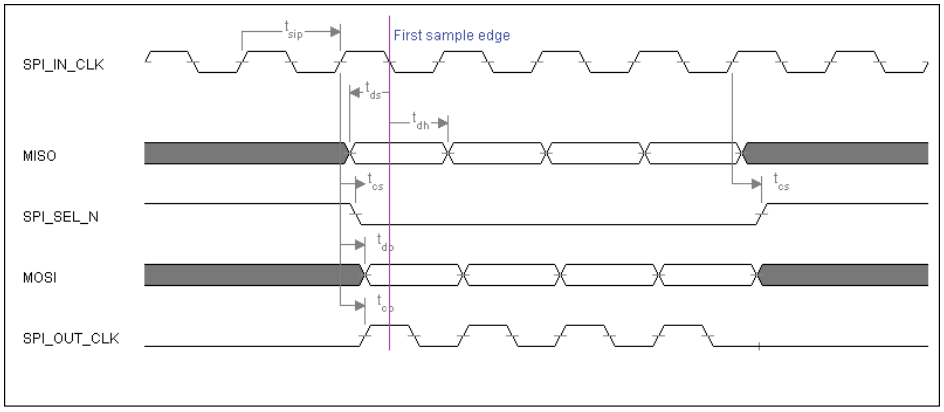


Figure 7-16. ClkSel = 1; RcvClkPol = 0; ClkPhase = 1; ClkPol = 1

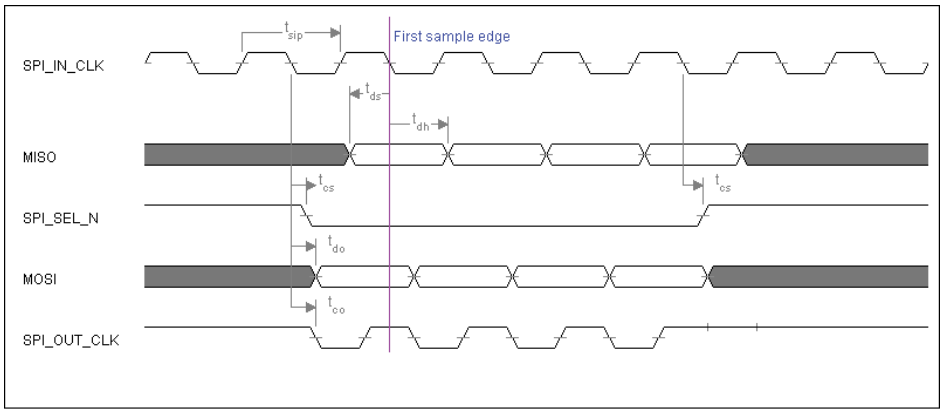


Figure 7-17. ClkSel = 1; RcvClkPol = 1; ClkPhase = 0; ClkPol = 0

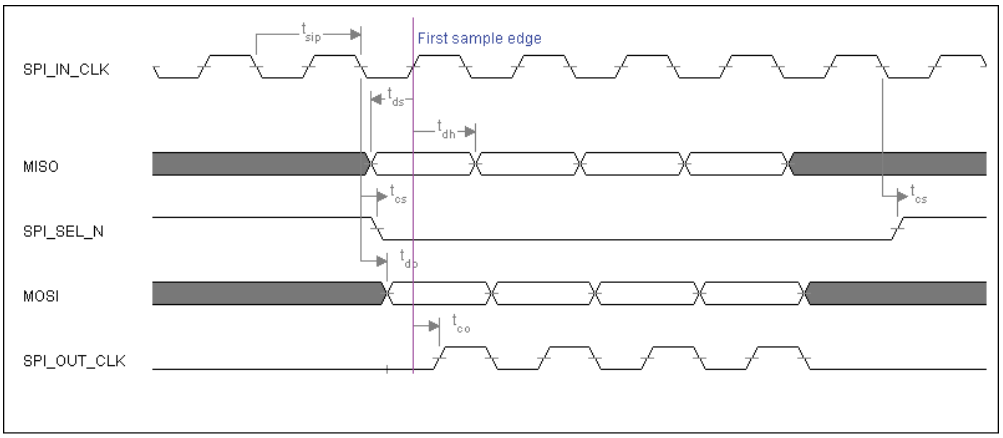


Figure 7-18. ClkSel = 1; RcvClkPol = 1; ClkPhase = 0; ClkPol = 1

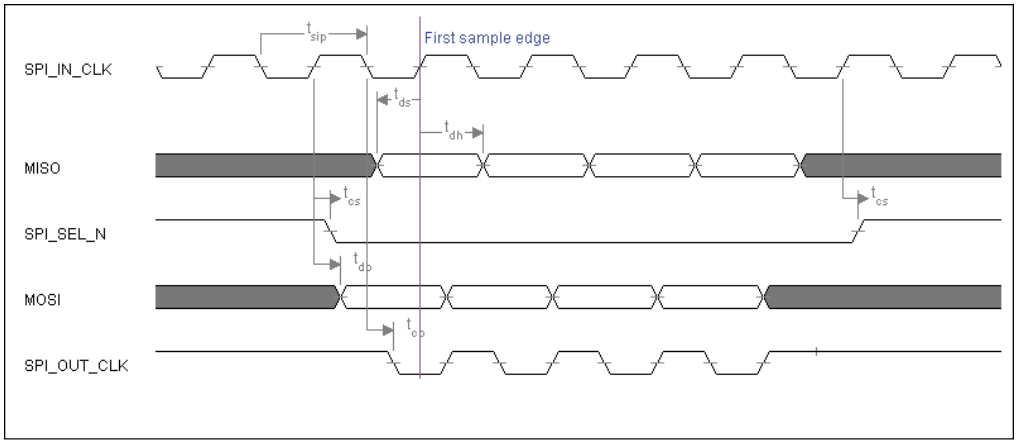


Figure 7-19. ClkSel = 1; RcvClkPol = 1; ClkPhase = 1; ClkPol = 0

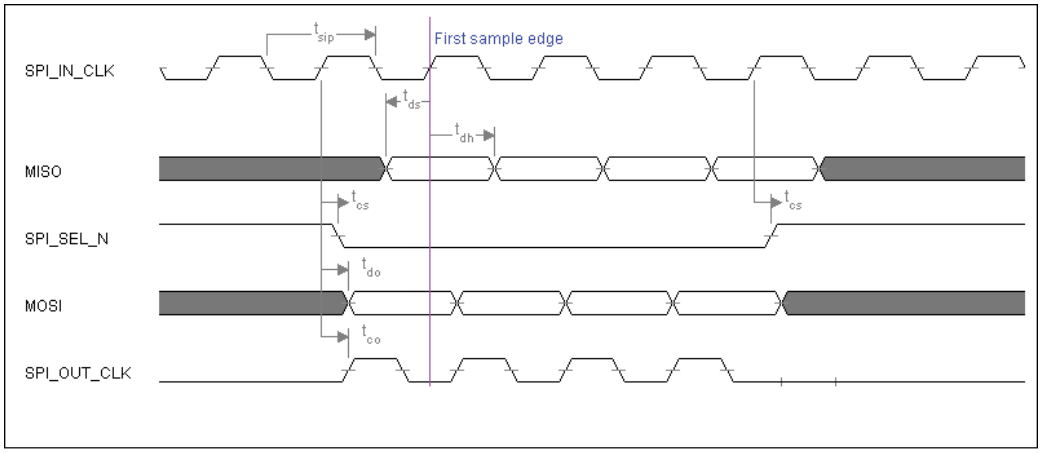


Figure 7-20. ClkSel = 1; RcvClkPol = 1; ClkPhase = 1; ClkPol = 1

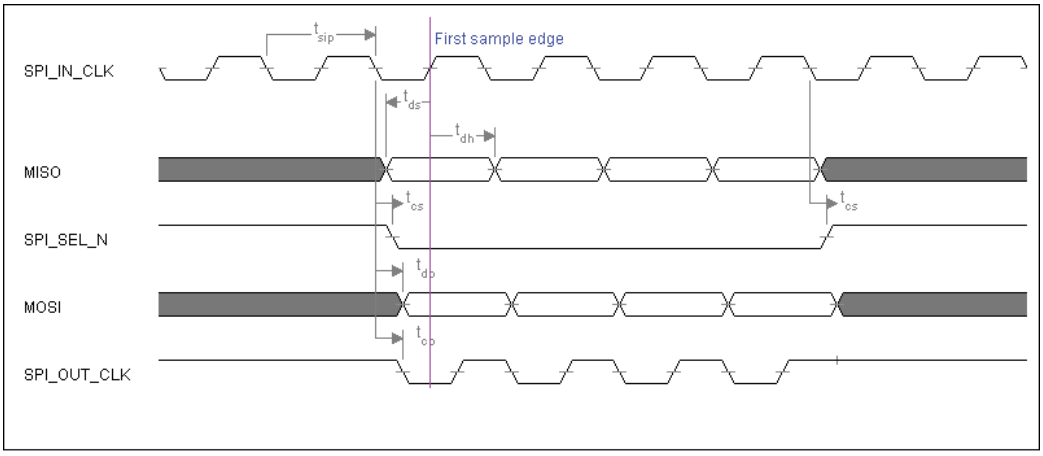


Table 7-23. Timing Parameters (External SPI Clock)

Symbol	Description	Min(ns)	Max(ns)
tsip	SPI_IN_CLK clock period	200	—
tds	MISO data setup	0	—
tdh	MISO data hold	tsys	—

.....continued

Symbol	Description	Min(ns)	Max(ns)
tcs	SPI_SEL_N delay	2 * tsys + 2	4 * tsys + 8.1
tdo	MOSI data output delay	3 * tsys + 2.8	6 * tsys + 7.2
tco	SPI_OUT_CLK output delay	3 * tsys + 3.1	6 * tsys + 8

7.7.6.2 Internal SPI Clock

Figure 7-21. ClkSel = 0; RcvClkPol = 0; ClkPhase = 0; ClkPol = 0

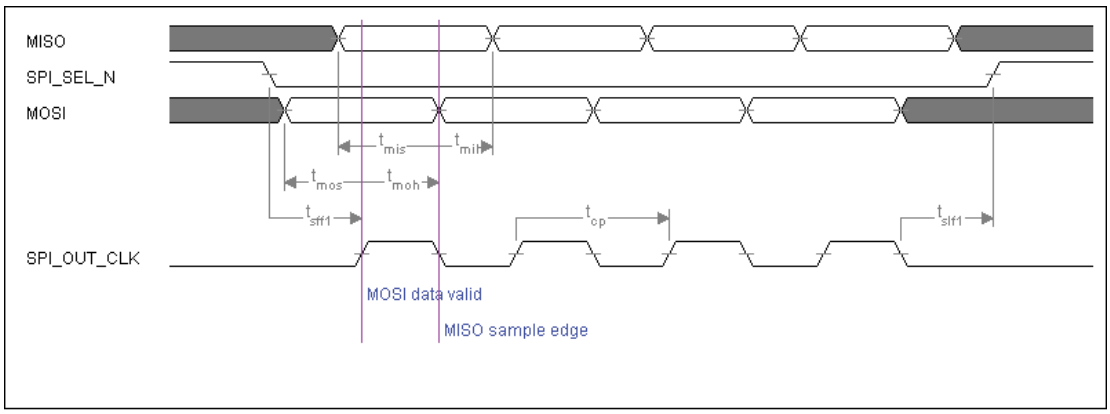


Figure 7-22. ClkSel = 0; RcvClkPol = 0; ClkPhase = 0; ClkPol = 1

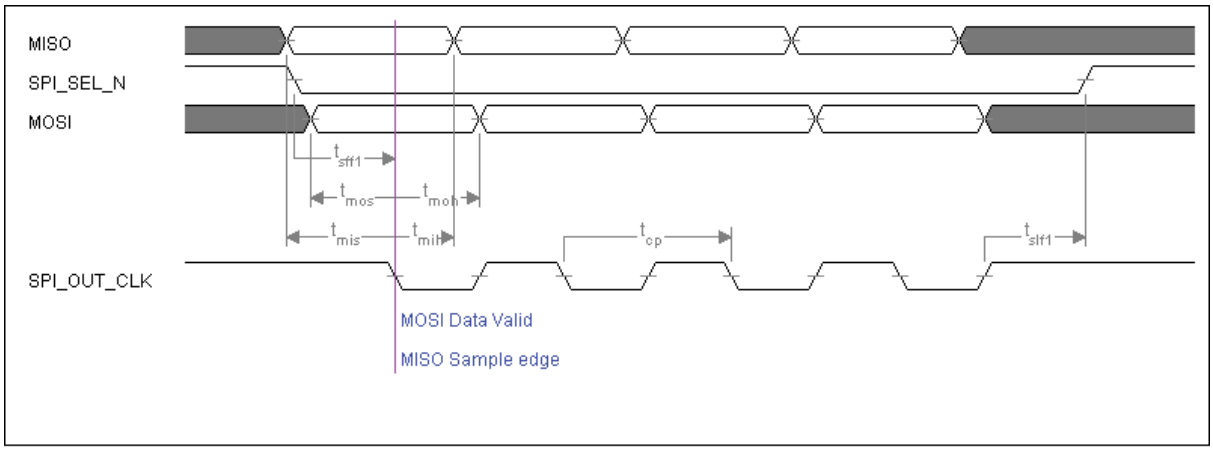


Figure 7-23. ClkSel = 0; RcvClkPol = 0; ClkPhase = 1; ClkPol = 0

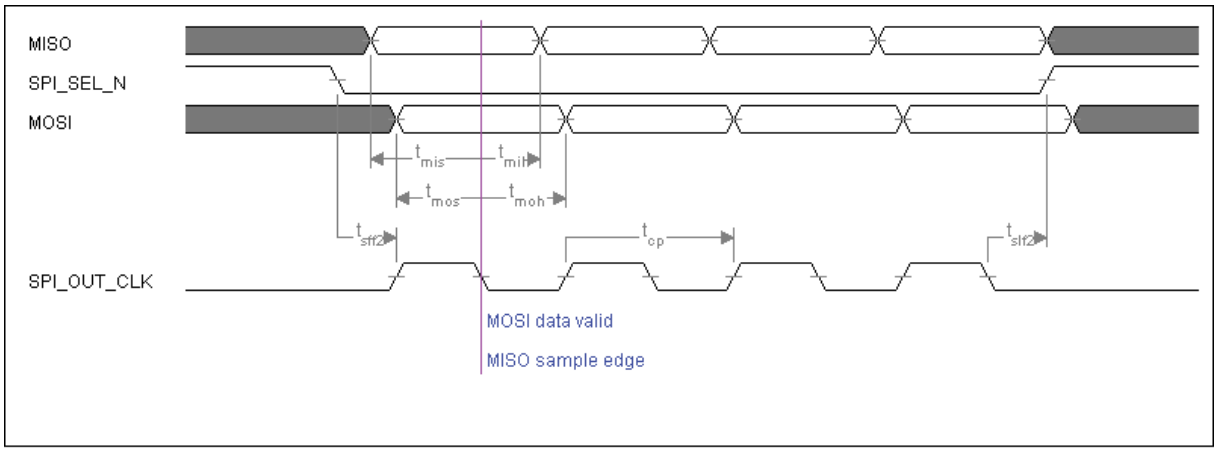


Figure 7-24. ClkSel = 0; RcvClkPol = 0; ClkPhase = 1; ClkPol = 1

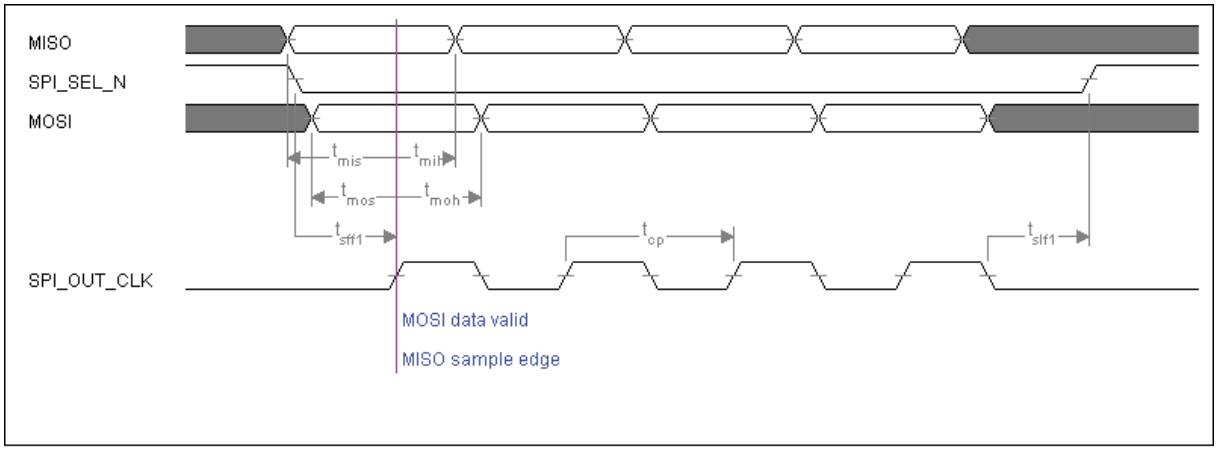


Figure 7-25. ClkSel = 0; RcvClkPol = 1; ClkPhase = 0; ClkPol = 0

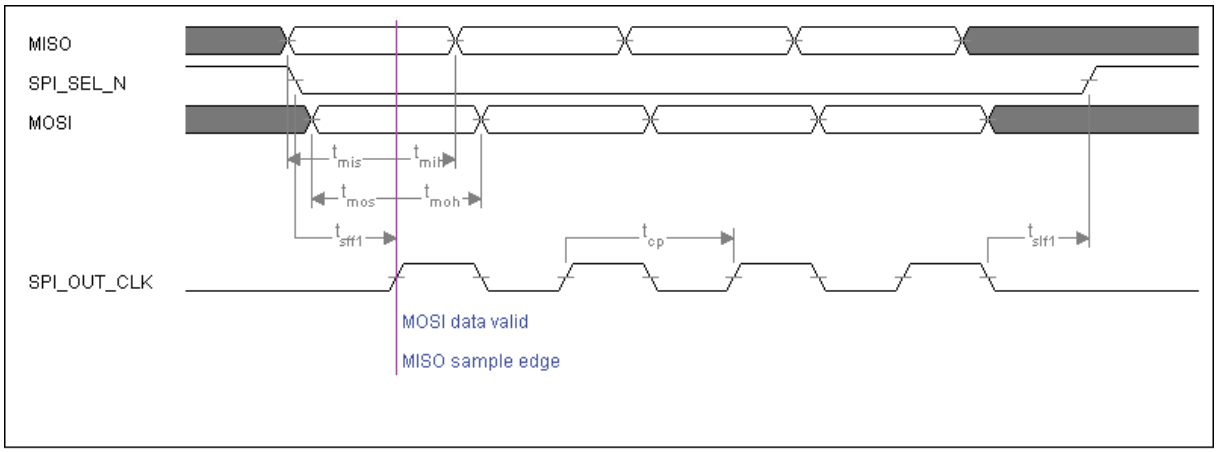


Figure 7-26. ClkSel = 0; RcvClkPol = 1; ClkPhase = 0; ClkPol = 1

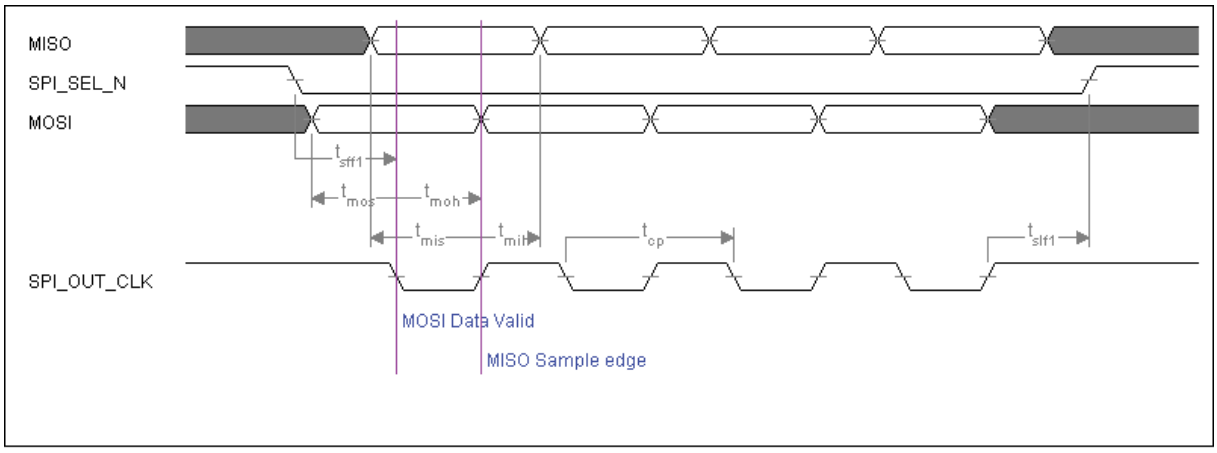


Figure 7-27. ClkSel = 0; RcvClkPol = 1; ClkPhase = 1; ClkPol = 0

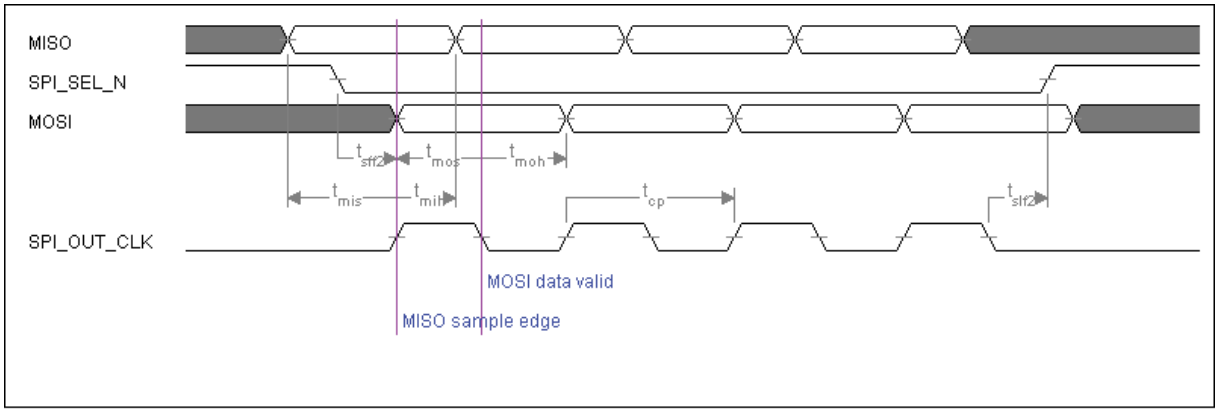


Figure 7-28. ClkSel = 0; RcvClkPol = 1; ClkPhase = 1; ClkPol = 1

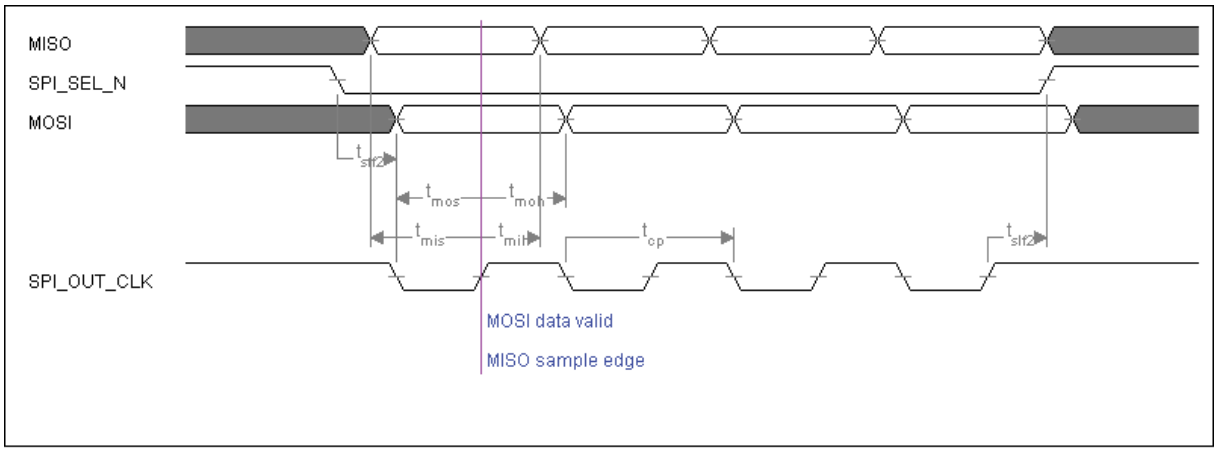


Table 7-24. Timing Parameters (Internal SPI Clock)

Symbol	Description	Min(ns)	Max(ns)
t_{SFF1}	SPI_SEL_N assertion to first SPI_OUT_CLK edge	(0.5* tcp)+ tsys-0.8	(0.5* tcp+tsys +0.9
t_{SLF1}	Last SPI_OUT_CLK edge to SPI_SEL_N deassertion	tcp- tsys-0.8	tcp- tsys+0.9
t_{SFF2}	SPI_SEL_N assertion to first SPI_OUT_CLK edge	3* tsys-0.8	3* tsys+0.9
t_{SLF2}	Last SPI_OUT_CLK edge to SPI_SEL_N deassertion	(0.5* tcp)- 1* tsys-0.8	(0.5* tcp)- 1* tsys+0.9
t_{MIS}	MISO setup time	4* tsys	—
t_{MIH}	MISO hold time	0	—
t_{MOS}	MOSI stable before SPI_OUT_CLK edge	0.5* tcp- tsys+0.2	0.5* tcp- tsys+0.7
t_{MOH}	MOSI hold after SPI_OUT_CLK edge	0.5* tcp-0.7	0.5* tcp+-0.2

8. Ordering Information

Ordering Code	Supply Voltage (core/los)	Temperature Range	Packaging	Quality flow
AT7991E-YF-E	1.8 V/3.3 V	25 °C	MQFP352	Engineering samples
AT7991E-YF-SV	1.8 V/3.3 V	-55 °C, 125 °C	MQFP352	Space Grade
AT7991E-YF-MQ	1.8 V/3.3 V	-55 °C, 125 °C	MQFP352	Military Grade

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